# Reliability Summary Report

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|---|---|
| Product Type: | 16Gb (1Gx16) DDR4 |
| | 16Gb (2Gx8) DDR4 |
| Part Number: | KTDMAG4B632BGCBA |
| | KTDMAG4B632BGIBA |
| | KTDMAG4B832BGCBA |
| | KTDMAG4B832BGIBA |
| Package: | 96 ball BGA |
| | 78 ball BGA |

# 1. Features

- Power supply (JEDEC standard 1.2V)
  - VDD = 1.2V ± 5%
  - VPP = 2.375V to 2.75V
- 16 internal banks – 16 banks (4 banks x 4 bank groups) for x8 product
- 8 internal banks - 8 banks (4 banks x 2 bank groups) for x 16 product
- Interface: Pseudo Open Drain (POD)
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- CAS Latency (CL): 10,(11),12,(13),14,(15),16,(17),18,19,20,22,24
- CAS Write Latency (CWL): 9,10,11,12,14,16,18,20
- On-Die Termination (ODT): nom. values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  Average refresh period
  - 7.8µs at 0°C ≤ TC ≤ +85°C or -40°C ≤ TC ≤ +85°C
  - 3.9µs at +85°C < TC ≤ +95°C
- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS_t and DQS_c) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation

- Data Bus Inversion (DBI)
  - Improve the power consumption and signal integrity of the memory interface (x16 product only)
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- VREFDQ training
  - VREFDQ generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)
  - Each DRAM can be set a different mode register value individually and has individual adjustment.
- Fine granularity refresh
  - 2x, 4x mode for smaller tRFC
- Programmable Partial Array Self-Refresh (PASR)
- RESET_n pin for power-up sequence and reset function
- Operating case temperature range:
  - Commercial: $T_C$ = 0°C to +95°C
  - Industrial: $T_C$ = -40°C to +95°C

# 2. Package Information

| Product No. | VDD | Data Rate (CL-tRCD-tRP) | Package | Temperature | Comments |
|---|---|---|---|---|---|
| KTDMAG4B632BGCBA | 1.2V | DDR4-3200 (22-22-22) | 96 ball BGA | Commercial | Pb-free |
| KTDMAG4B632BGIBA | 1.2V | DDR4-3200 (22-22-22) | 96 ball BGA | Industrial | Pb-free |
| KTDMAG4B832BGCBA | 1.2V | DDR4-3200 (22-22-22) | 78 ball BGA | Commercial | Pb-free |
| KTDMAG4B832BGIBA | 1.2V | DDR4-3200 (22-22-22) | 78 ball BGA | Industrial | Pb-free |

**Note:**

The above description is extracted from the datasheet. Please refer to the document for detailed information.

# 3. Product Qualification Tests

## 3.1. Enviromental Tests

| No. | Item | Condition | Sample Size | Results |
|---|---|---|---|---|
| 1 | Pre-Conditioning | JESD22-A113/JESD-020 (MSL 3) (bake 24h+TH 60°C/60% 52h+reflow 3x) | 304 | Passed |
| 2 | TC (Temperature Cycling) | JESD-22-A104E (-55C° to 125C°, no bias), up to 600 cycles | 76 | Passed |
| 3 | THB (Temperature & Humidity with Bias) | JESD22-A101D (85°C/85% with bias), up to 1000h | 76 | Passed |
| 4 | uHAST | JESD22-A111B (130C°/85%/1 atm, no bias), up to 168h | 76 | Passed |
| 5 | HTS (High Temperature Storage) | JESD22-A103E (150°C, no bias), up to 1000h | 76 | Passed |
| 6 | MSL Reclassification | JESD-020, MSL3 (SAT+bake 24h+TH 60°C/60% 52h+reflow 3x+SAT) | 33 | Passed |

## 3.2. Operating, ESD & Latch-up Tests

| No. | Item | | Condition | Sample Size | Results |
|---|---|---|---|---|---|
| 1 | High Temperature Operating Life (HTOL) | | JESD22-A108F (125°C, Dynamic Stress) up to 300h | 76 | Pass |
| 2 | Low Temperature Operating Life (LTOL) | | JESD22-A108F (-10°C, Dynamic Stress) up to 300h | 76 | Pass |
| 3 | ESD | HBM | JESD-A114F (2kV) | 40 | Pass |
| | | CDM | JESD22-C101F (500V) | 30 | Pass |
| 4 | Latch-Up | V-test | JESD78E (6V/2.94V) | 10 | Pass |
| | | I-test | JESD78E (150mA) | 40 | Pass |