SMARTsemi
Memory IC Datasheet

Industrial Grade eMMC 153b

November 2022
Rev 0.5

REVISION HISTORY

Date	Revision	Section(s)	Description
May 2022	0.1	All	Preliminary Release
July 2022	0.2	Endurance, Register	Update Endurance notes and Register
Sep. 2022	0.3	All	Add 16GB part number and its information
Sept. 2022	0.4	Register	Update ECSD Register info
Nov. 2022	0.5	Register	Update ECSD Register info

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 GENERAL DESCRIPTION

1.1 Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, Global wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMARTsemi's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

1.2 Features

- Industrial Standard Interface
  - JEDEC / eMMC Standard Version 5.1 Compliant

- eMMC 5.1 Enhanced Features
  - 12-signal interface (including CMD, CLK, DAT[7:0], DS, and RST_n)
  - Programmable bus width: 1-bit, 4-bit, and 8-bit
  - Supports HS400 high speed interface timing mode up to 400MB/s data rate
  - Up to 200MHz clock frequency
  - Supports eMMC Field firmware update (FFU)
  - Supports eMMC device health report
  - High-speed, Dual Data Rate support
  - Supports Boot and Alternative Boot Mode
  - Replay Protected Memory Block (RPMB)
  - Trim, Secure Erase, Sanitize
  - Enhanced Partition Attributes
  - High Priority Interrupt (HPI)
  - Background Operations
  - Enhanced Reliable Write
  - Supports Enhanced Strobe in HS400 Mode
  - Supports eMMC Background Operation Control

- Robust Data Protection and Endurance
  - Internal error correction code (ECC) to protect data communication
  - Enhanced Write Protection with Permanent and Partial protection options
  - Wear-Leveling and early block failure monitoring/retirement ensure the data reliability
  - Solid protection of sudden power failure safe-update operations for data content

- Supply Voltage
  - eMMC Interface Power (VCCQ): 1.70-1.95V
  - eMMC Interface Power (VCCQ): 2.7-3.6V[1]
  - NAND Memory Power (VCC): 2.7-3.6V

- MLC NAND
  - 153-ball standard BGA packages
  - Green Package and RoHS Compliant

- Operating Temperature
  - Industrial Grade: -40°C ~ +85°C

- Secure Erase
  - Support secure erase and trim commands

Note: [1] HS200 and HS400 mode are not supported when VCCQ is in 2.7-3.6V.

2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Table

Normal Memory

Native Capacity	User Capacity	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB	8GB (MLC mode)	240	110	3100	4100
16GB	16GB (MLC mode)	240	110	3100	4100

(1) Test condition: GL3227 Card Reader, USB3.0, FAT32 File System, Intel i5 3.5GHz, 8GB DDR3 @25℃

2.2 Power Consumption

Table 2: Current Consumption

Mode	Capacity	Icc (MAX)	Iccq (MAX)
Active	8GB	100mA	130mA
	16GB	100mA	130mA
Standby	8GB	50uA	120uA
	16GB	70uA	150uA

Notes:

(1) Power measurement condition: HS400, 25C, Vcc=3.3V, Vccq=1.8V

2.3 Data Reliability

- **Global Wear Leveling:** To achieve the best stability and device endurance, this eMMC equips the Global Wear Leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.
- **ECC**: The hardware error correction code (ECC) function, which can prevent data corruption, is included in the eMMC controller.
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

2.4 Environmental Conditions

Table 3: Environmental Conditions and Test Conditions

Parameter	Value
Operating Temperature	-40°C to 85°C
Storage Temperature	-40°C to 85°C

2.5 Endurance[1]

Table 4: Reliability Characteristics

Item	Value	
Data Retention (@ 55˚C)	10 years when 90% life remaining	
	1 year when 10% life remaining	
100% Sequential Workload	8GB	12 TBW
	16GB	24 TBW

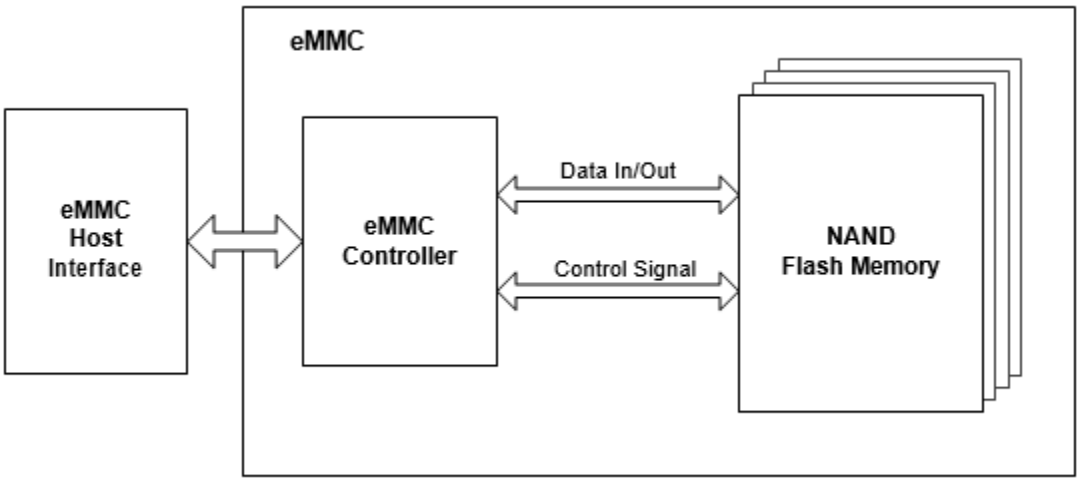
[1] Endurance is directly related to the User specific workload.

3 PRODUCT DESCRIPTION

The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

3.1 Functional Block Diagram

Figure 1: eMMC Block Diagram

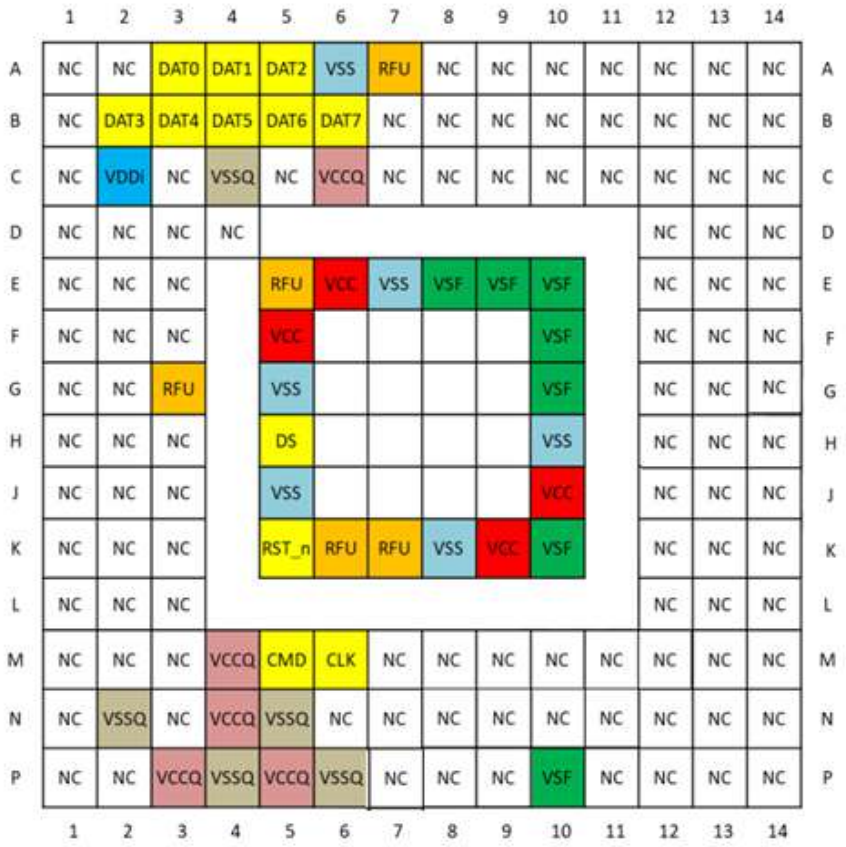


4 PACKAGE INFORMATION

4.1 Signal Interface

4.1.1 eMMC Ball-out Diagram

Figure 2: 153-Ball Pin Assignments (Top View, Balls Down)*



*RFU: Reserved for future use; VSF: Vendor specific function; It is not good for layout other signal traces via or on these pins.

4.1.2 Signal Descriptions

Table 5: Signal Descriptions

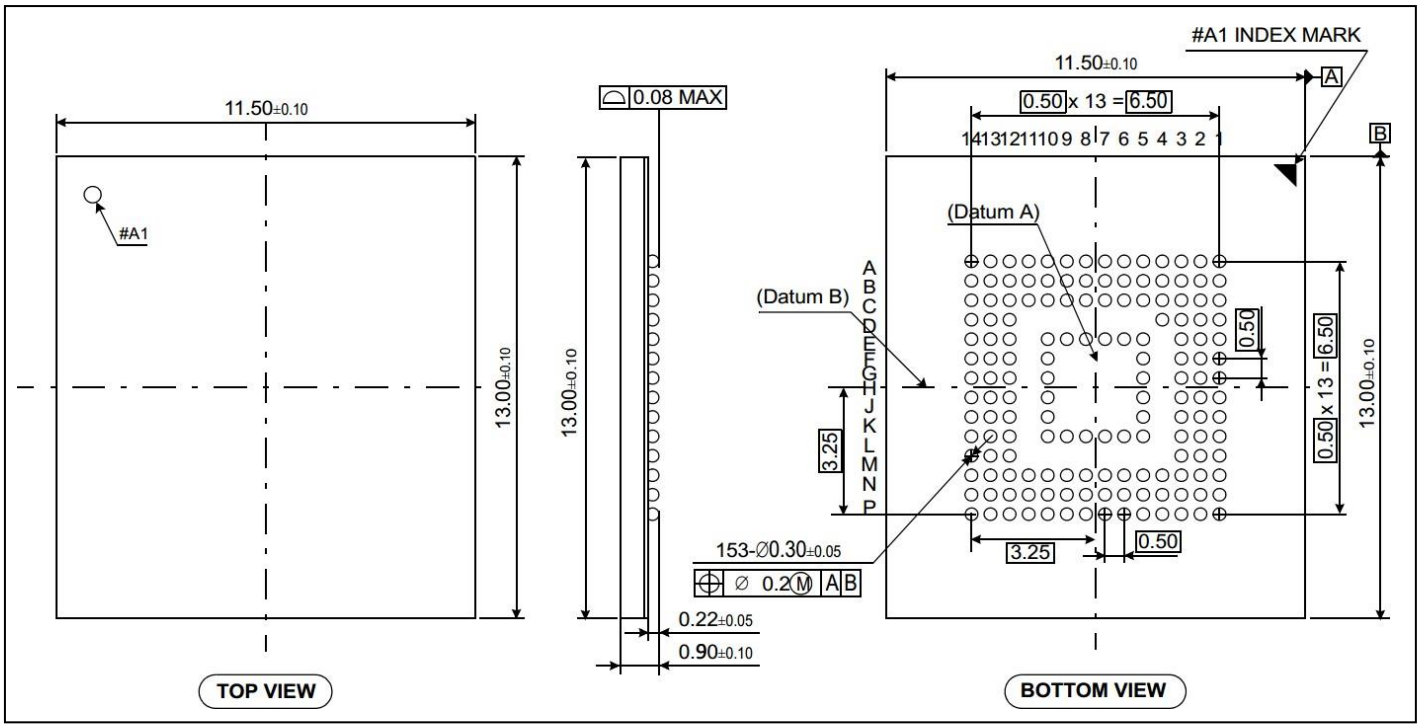
Pin No.	Pin Name	Description
A3	DAT0	These are bidirectional data signal. The DAT signals operate in push-pull mode. Only the device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the device disconnects the internal pull-ups of lines DAT1–DAT7
A4	DAT1	
A5	DAT2	
B2	DAT3	
B3	DAT4	
B4	DAT5	
B5	DAT6	
B6	DAT7	
K5	RSTN	Hardware Reset Input
C6	VCCQ	VCCQ is the power supply line for host interface, have two power mode: High power mode:2.7V~3.6V; Lower power mode: 1.7V~1.95V.
M4	VCCQ	
N4	VCCQ	
P3	VCCQ	
P5	VCCQ	
E6	VCC	VCC is the power supply line for internal flash memory, its power voltage range is:2.7V~3.6V.
F5	VCC	
J10	VCC	
K9	VCC	
C2	VDDi	VDDi is internal power node, not the power supply. Connect 1uF capacitor VDDi to ground.
M5	CMD	This signal is a bidirectional command channel used for device initialization and command transfer. Commands are sent from the host to the device, and responses are sent from the device to the host. The CMD Signal has 2 operation modes: open drain for initialization, and push-pull for command transfer.
H5	DS	Data Strobe signal. Newly assigned pin for HS400 mode. Data Strobe is generated from eMMC to host. In HS400 mode, read data and CRC response are synchronized with Data Strobe.
M6	CLK	Each cycle of this signal directs a one-bit transfer on the command and either a one-bit (1x) or a two-bits transfer (2x) on all the data lines.

Pin No.	Pin Name	Description
J5	VSS	Ground connections
A6	VSS	
C4	VSS	
E7	VSS	
G5	VSS	
H10	VSS	
K8	VSS	
N2	VSS	
N5	VSS	
P4	VSS	
P6	VSS	

5 EMMC MECHANICAL SPECIFICATION

5.1 Package Dimensions

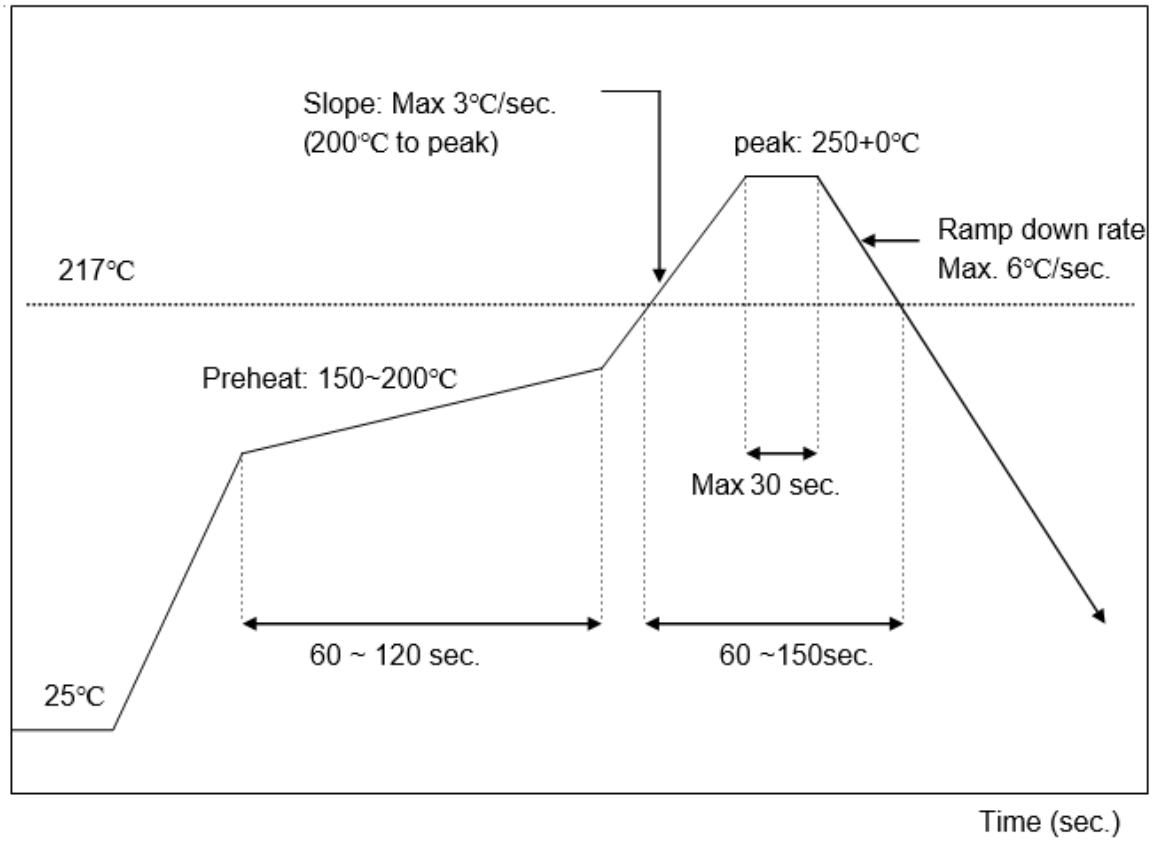
Figure 3: 153-Ball BGA Dimensions – 11.5 mm x 13 mm



5.2 Recommended Reflow Profiles

Table 6: Recommended Reflow Profile

Reflow Parameters	Suggested Range
Specifications:	IPC/JEDEC J-STD-020E
Average ramp-up rate (200℃ to peak):	3 ℃/sec. max
Preheat:	150~200℃, 60~120 seconds
Temperature maintained above 217℃:	60~150 seconds
Time within 5℃ of actual peak temperature:	10~30 seconds
Peak temperature:	250+0℃
Ramp-down rate:	6℃/sec. max.
Time 25℃ to peak temperature:	480 sec. max.



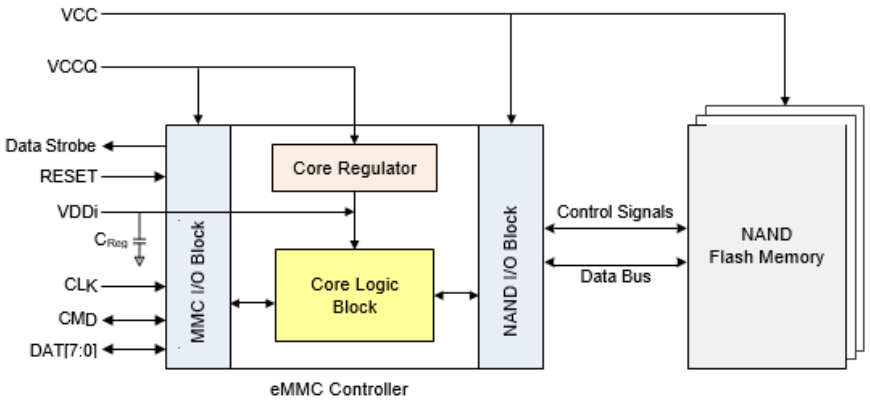
6 ELECTRICAL SPECIFICATION

6.1 Electrical Interface

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device voltage; V_{CCQ} is used for the controller and the eMMC interface voltage.

Figure 4: System Architecture

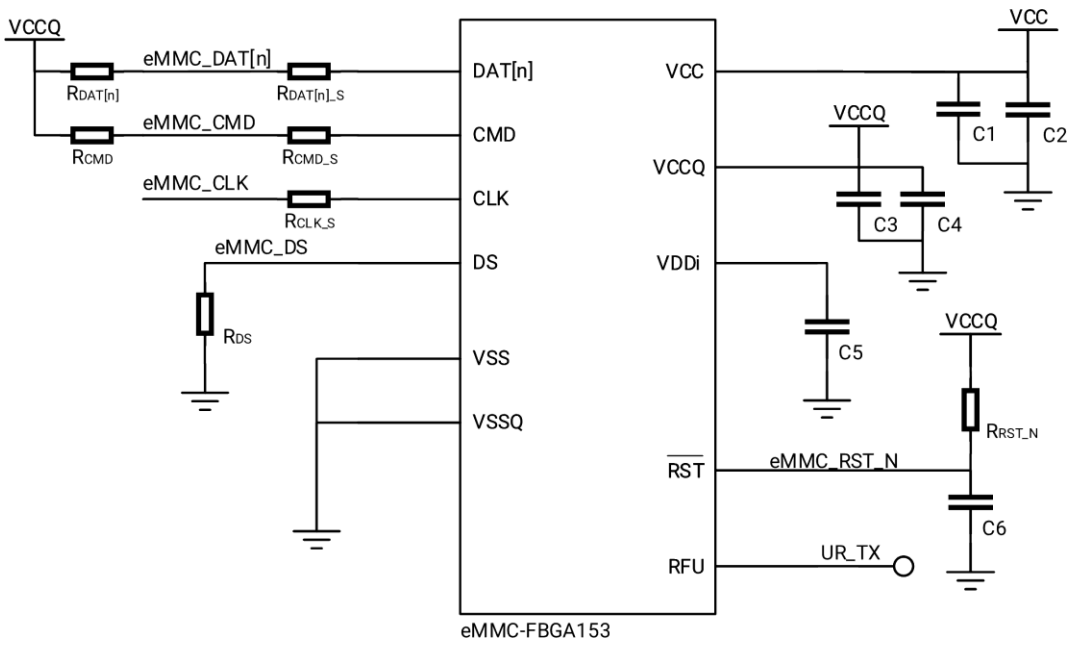


6.2 DC Specifications

Table 7: Power Requirements

Parameter	Symbol	Min	Typical	Max	Remark
Power of VCC	VCC	2.7V	3.3V	3.6V	Should be separated from VCCQ
Power of VCCQ (High Perf.)	VCCQ	1.7V	1.8V	1.95V	HS200/HS400
Power of VCCQ (Low Perf.)	VCCQ	2.7V	3.3V	3.6V	52MHz CLK SDR/DDR
DAT[n] Pull-Up Resistance	RDAT[n]	10kΩ	--	100kΩ	DAT[n], n=0~7
CMD Pull-Up Resistance	RCMD	4.7kΩ	--	100kΩ	
DS Pull-Down Resistance	RDS	10kΩ	--	100kΩ	HS200/HS400
RST_N Pull-Up Resistance	RRST_N	--	NC	--	Reserving for EVT
DAT[n] Serial Resistance	RDAT[n]_S	--	0Ω	33Ω	Reserving for EVT
CMD Serial Resistance	RCMD_S	--	0Ω	33Ω	Reserving for EVT
CLK Serial Resistance	RCLK_S	--	0Ω	33Ω	Reserving for EVT
Power Coupling Capacitor 1	C1, C3	2.2μF	--	4.7μF	6.3V, X5R or higher classification
Power Coupling Capacitor 2	C2, C4	--	0.1μF	--	6.3V, X5R or higher classification
VDDi Coupling Capacitor	C5	0.1μF	1μF	--	6.3V, X5R or higher classification
RST_N Coupling Capacitor	C6	--	NC	--	6.3V, X5R or higher classification

Figure 5: Recommended eMMC Connection



Note:

1) Coupling capacitor should be connected with VCC/VCCQ and VSS as closely as possible.
2) The VCC and VCCQ power should be separated.
3) Lay the VSS between the CLK and the Data lines.

7 REGISTER

The registers used in the SMART eMMC are shown in the table below. These registers are described in the sections that follow:

Table 8: Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

7.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 9: CID Register Field Parameters

Name	Field	Width (Bits)	CID Bits	SMART CID Value	
Manufacturer ID	MID	8	[127:120]	0xF6	
Reserved	-	6	[119:114]	--	
Device / BGA	CBX	2	[113:112]	0x01	
OEM/application ID	OID	8	[111:104]	0x00	
Product name	PNM	48	[103:56]	8GB	8GL1A
				16GB	AGL1A
Product revision	PRV	8	[55:48]	0x10	
Product serial number	PSN	32	[47:16]	--(1)	
Manufacturing date	MDT	8	[15:8]	--(2)	
CRC7 checksum	CRC	7	[7:1]	--(3)	
reserved	-	1	0	--	

Note:

(1) Unique for each device. 32-bit unsigned binary integer.
(2) 2 hex digits for device manufacturing month and year.
(3) CRC for CID register. Different for each device.

7.2 OCR Register

The card identification (OCR) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 10: OCR Register Field Definitions

V_{DD} Voltage Window	Width (Bits)	OCR Bits	OCR Value
Ready/Busy	1	[31]	card power up status bit (busy)(1)
Access Mode	2	[30:29]	10b
Reserved	5	[28:24]	0 0000b
2.7-3.6V	9	[23:15]	1 1111 1111b
2.0-2.6V	7	[14:8]	000 0000b
1.70-1.95V	1	[7]	1b
Reserved	7	[6:0]	000 0000b

Note:

(1) This bit is set to low if the device has not finished the power up routine.

7.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 11: CSD Register Field Parameters

Name	Field	Width (Bits)	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	[127:126]	0x03
System specification version	SPEC_VERS	4	[125:122]	0x04
Reserved	-	2	[121:120]	--
Data read access time 1	TAAC	8	[119:112]	0xFF
Data read access time 2 in CLK cycles (NSAC x 100)	NSAC	8	[111:104]	0xFF
Maximum bus clock frequency	TRAN_SPEED	8	[103:96]	0x32
Device command classes	CCC	12	[95:84]	0x9F5
Maximum read data block length	READ_BL_LEN	4	[83:80]	0x09
Partial blocks for reads supported	READ_BL_PARTIAL	1	[79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0x00
DSR implemented	DSR_IMP	1	[76]	0x00
Reserved	-	2	[75:74]	--
Device size	C-SIZE	12	[73:62]	0xFFF
Maximum read current as VDD,min	VDD_R_CURR_MIN	3	[61:59]	0x07
Maximum read current as VDD,max	VDD_R_CURR_MAX	3	[58:56]	0x07
Maximum write current as VDD,min	VDD_W_CURR_MIN	3	[55:53]	0x07
Maximum write current as VDD,max	VDD_W_CURR_MAX	3	[52:50]	0x07
Device size multiplier	C-SIZE_MULT	3	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	[31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0x00
Write-speed factor	R2W_FACTOR	3	[28:26]	0x05
Maximum write data block length	WRITE_BL_LEN	4	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0x00
Reserved	-	4	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	[16]	0x00
File-format group	FILE_FORMAT_GRP	1	[15]	0x00

Name	Field	Width (Bits)	CSD Bits	CSD Value
Copy flag (OTP)	COPY	1	[14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0x00
Temporary write protection	TEMP_WRITE_PROTECT	1	[12]	0x00
File format	FILE_FORMAT	2	[11:10]	0x00
ECC code	ECC	2	[9:8]	0x00
CRC	CRC	7	[7:1]	--
Not used; always 1	-	1	[0]	--

7.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 12: ECSD Register Field Parameters

Name	Field	Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Reserved	-	6	-	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported command sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x03
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES	1	R	[493]	0x03
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0x00
Barrier support	BARRIER_SUPPORT	1	R	[486]	0X00
Reserved	-	181	-	[485:309]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	-
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	Variable
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	Variable
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x00
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x20
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device version	Device version	2	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0x0000 0000 0003 0502
Power class for200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x00010000
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x0A
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache Flushing Policy	CACHE_FIUSH_POLICY	1	R	[240]	0x00
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200 MHz at 1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200 MHz at 1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved	-	1	-	[233]	--
TRIM multiplier	TRIM_MULT	1	R	[232]	0x05
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
SECURE ERASE multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
SECURE TRIM multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved	-	1	-	[227]	--
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	6h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x05
Reliable write-sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x07
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x00
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x16
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x10
Sector count	SEC-COUNT	4	R	[215:212]	8GB: E40000h 16GB: 1CC8000h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved	-	1	-	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x0A
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x05
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card type	CARD_TYPE	1	R	[196]	0x57
Reserved	-	1	-	[195]	--
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	-	1	-	[193]	--
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	-	1	-	[190]	--
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	-	1	-	[188]	--
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	-	1	-	[186]	--
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved	-	1	-	[182]	--
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved	-	1	-	[180]	--
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved	-	1	-	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	0x00
Reserved	-	1	-	[172]	--
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	-	1	-	[170]	--
Firmware configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x15
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
Hardware reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	0x07
Maximum enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	8GB: 0x0001C8 16GB: 0x000399
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h
Partitioning setting	PARTITIONING_SETTING-COMPLETED	1	R/W	[155]	0h
General-purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0h
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved	-	1	-	[135]	--

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved	-	2	-	[129:128]	--
Vendor specific fields	VENDOR_SPECIFIC_NFIELD	64	<vs>	[127:64]	-
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 command control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved	-	2	-	[28:27]	--
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATASIZE	4	R	[21:18]	-
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x00
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x09
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved	-	15	-	[14:0]	-

Notes:

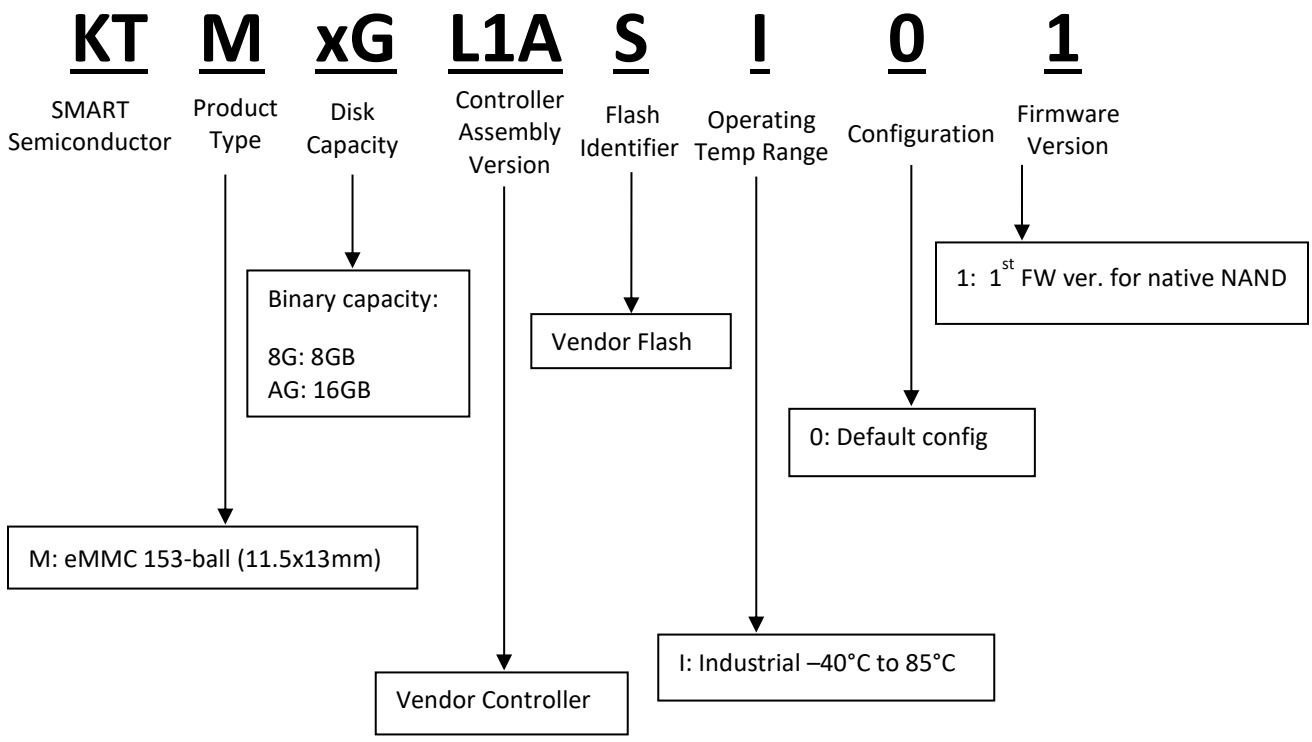
1. The definitions of cell type are shown as follows:
   R: Read only.
   W: One time programmable and not readable.
   R/W: One time programmable and readable.
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable. R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable. W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.
2. Reserved bits should be read as “0”.
3. The column marked with “-“ is undefined.

8 PART NUMBERS

Table 13: Part Numbering Information

Capacity	Part Number
8GB	KTM8GL1ASI01
16GB	KTMAGL1ASI01

8.1 Part Number Decoder



Disclaimer:

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of SMART Semiconductor. ("SMARTsemi"). The information in this document is subject to change without notice. SMARTsemi assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SMARTsemi makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems, and life support systems. Moreover, SMARTsemi does not recommend or approve the use of any of its products in life support devices or systems, or in any application where failure could result in injury or death. If a customer wishes to use SMARTsemi products in applications not intended by SMARTsemi, said customer must contact an authorized SMARTsemi representative to determine SMARTsemi's willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks, or other intellectual property rights claimed and owned by SMARTsemi. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SMARTsemi.

ALL PRODUCTS SOLD BY SMARTSEMI ARE COVERED BY THE PROVISIONS APPEARING IN SMARTSEMI'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY, AND INFRINGEMENT PROVISIONS. SMARTSEMI MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED, OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT, AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY, OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.