



SMARTsemi

Memory IC Datasheet

Automotive Grade eMMC 153b

March 2023
Rev 0.2

REVISION HISTORY

Date	Revision	Section(s)	Description
December 2022	0.1	All	Initial Release
March 2023	0.2	Cover Page	Update Temperature Grade



ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1 GENERAL DESCRIPTION

1.1 Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, Wear leveling algorithms, and other data management techniques provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMARTsemi's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

1.2 Features

- Industrial Standard Interface
 - JEDEC / eMMC Standard Version 5.0 Compliant
- eMMC 5.0 Enhanced Features
 - 12-signal interface (including CMD, CLK, DAT[7:0], DS, and RST_n)
 - Supports three data bus widths: 1-bit (default), 4-bits, and 8-bits
 - Supports HS400 high speed interface timing mode up to 400MB/s data rate
 - Up to 200MHz clock frequency
 - Supports eMMC Field firmware update (FFU)
 - Cache barrier
 - High-speed, Dual Data Rate support
 - BKOPS control
 - Improved RPMB throughput
 - Trim, Secure Erase
 - Enhanced write protection with permanent and partial protection options
 - Power off notification
 - Pre EOL information
 - Enhanced device lifetime
 - Optimal size
 - Cache flushing report
- Robust Data Protection and Endurance
 - Internal error correction code (ECC) to protect data communication
 - Enhanced Write Protection with Permanent and Partial protection options
 - Internal enhanced data management algorithm

- Protection from sudden power failure of safe-update operation for data content
- Supply Voltage
 - eMMC Interface Power (VCCQ): 1.70-1.95V
 - eMMC Interface Power (VCCQ): 2.7-3.6V¹
 - NAND Memory Power (VCC): 2.7-3.6V
- MLC NAND
 - 153-ball standard BGA packages
 - Green Package and RoHS Compliant
- Operating Temperature
 - Automotive (Wide) Grade: -40°C to +105°C
- Secure Erase
 - Support secure erase and trim commands

Note: ¹ HS200 and HS400 mode are not supported when VCCQ is in 2.7-3.6V.

2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Table

Normal Memory (HS400)

Capacity	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB	260	85	5800	2100
16GB	260	130	6000	2200
32GB	260	130	6000	2200

(1) Test condition: Cache is off

(2) Test condition: Testmetrix VTESA-4100E; bus in x8 I/O mode.

2.2 Power Consumption

Table 2: Current Consumption

Condition1		ICC/ICCQ (Typical)			Units
		8GB (native)	16GB (native)	32GB (native)	
Write	DDR52	35/75	65/85	95/100	mA
	HS200	35/75	65/85	125/125	mA
	HS400	35/75	65/85	125/125	mA
Read	DDR52	20/120	20/130	20/130	mA
	HS200	30/145	30/155	30/155	mA
	HS400	40/185	40/195	40/200	mA
Sleep current		110	115	125	μA
Standby		45/165	55/175	85/190	μA

(1) Bus in x8 I/O mode; 25°C; VCCQ = 1.8 V in HS200 and HS400 VCCQ = 3.3V in DDR52. Measurements done as maximum RMS current consumption over 100 milliseconds.

2.3 Data Reliability

- **Wear Leveling:** Efficient algorithms prolong the life of NAND by monitoring the cells in the device.
- **ECC:** The hardware error correction code (ECC) function, which can prevent data corruption, is included in the eMMC controller.
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

2.4 Environmental Conditions

Table 3: Environmental Conditions and Test Conditions

Parameter	Value
Operating Temperature	-40°C to 105°C
Storage Temperature	-40°C to 105°C

2.5 Endurance¹

Table 4: Reliability Characteristics

Item	Value	
Data Retention (@ 45°C)	10 years when 95% life remaining	
	1 year when 10% life remaining	
100% Sequential Workload	8GB	10 TBW
	16GB	24 TBW
	32GB	56 TBW

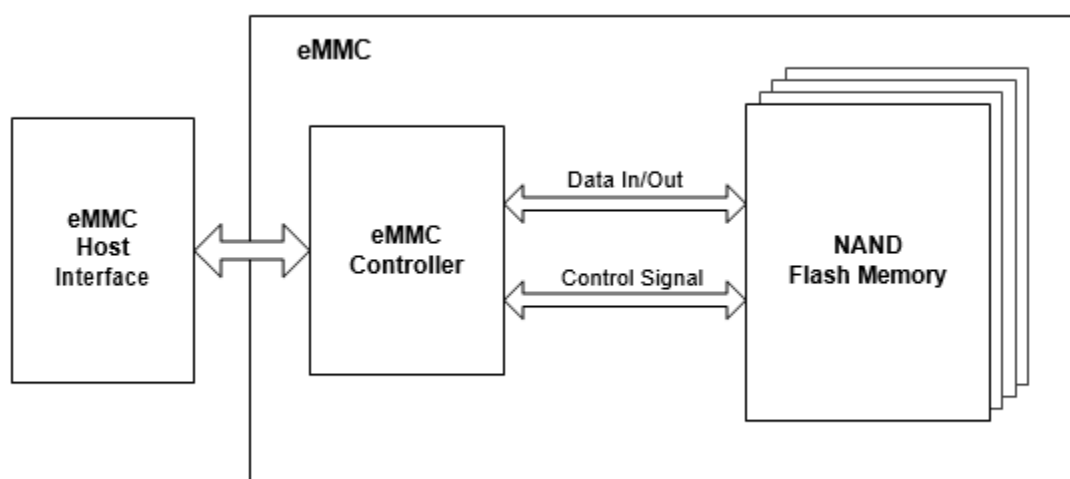
¹ Endurance is directly related to the User specific workload.

3 PRODUCT DESCRIPTION

The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

3.1 Functional Block Diagram

Figure 1: eMMC Block Diagram



4 PACKAGE INFORMATION

4.1 Signal Interface

4.1.1 eMMC Ball-out Diagram

Figure 2: 153-ball Pin Assignments (Top View, Balls Down)*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDI	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		VCC					VSF		NC	NC	NC	F
G	NC	NC	RFU		VSS					VSF		NC	NC	NC	G
H	NC	NC	NC		DS					VSS		NC	NC	NC	H
J	NC	NC	NC		VSS					VCC		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	VSS	VCC	VSF		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	RFU	NC	NC	VSF	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

*RFU: Reserved for future use; VSF: Vendor specific function; Do not layout other signal traces via or on these pins.

4.1.2 Signal Descriptions

Table 5: Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock Signal.
RST_n	Input	Hardware Reset Signal.
CMD	I/O	Command Signal.
DAT[7:0]	I/O	Data Bus.
DS	Output	Data Strobe Signal, Used in HS400 mode.
V _{CC}	Supply	Supply voltage for controller and Flash memory power.
V _{CCQ}	Supply	Supply voltage for controller and eMMC I/O power.
V _{SS}	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
V _{SSQ}	Supply	Supply voltage ground for controller and IO Flash memory. Can be short with VSS.
V _{DDi}		Connect capacitor from VDDi to GND for stabilize internal power.
NC	-	In eMMC chip is no connect. Left it floating.
RFU	-	Reserved for future use. Left floating for future use.
VSF	-	Vendor Specific Function. Reserved for test points on the PCB, default NU (Not Used)

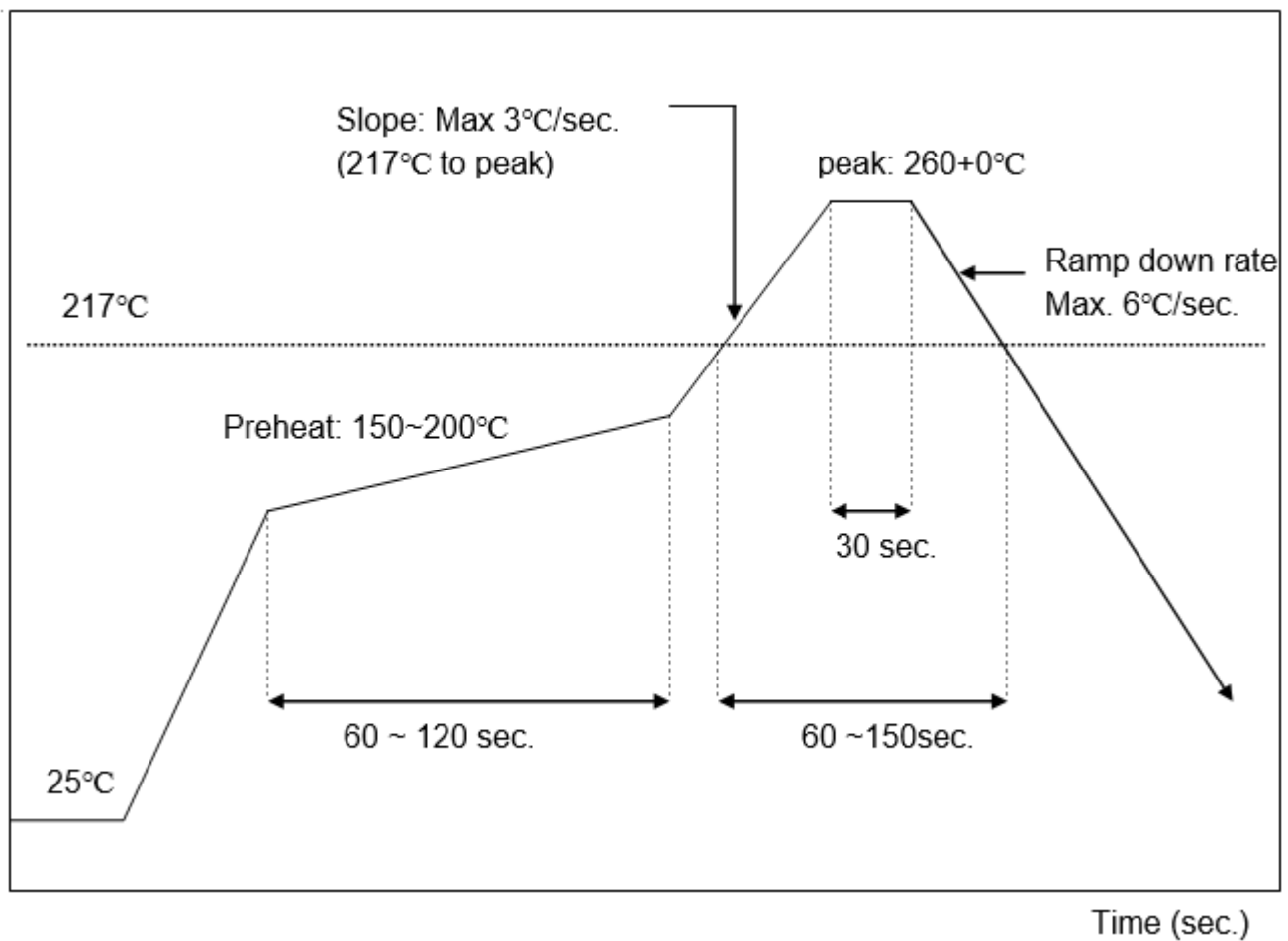
Some balls can be floated to achieve forced eMMC 4.5 conversion.

- A6 VSS → Float NC
- J5 VSS → Float NC
- H5 DS → Float NC

5.2 Recommended Reflow Profiles

Table 6: Recommended Reflow Profile

Reflow Parameters	Suggested Range
Specifications:	IPC/JEDEC J-STD-020E
Average ramp-up rate (200°C to peak):	3 °C/sec. max
Preheat:	150~200°C, 60~120 seconds
Temperature maintained above 217°C:	60~150 seconds
Time within 5°C of actual peak temperature:	255~260°C, 30 seconds
Peak temperature:	260+0°C
Ramp-down rate:	6°C/sec. max.
Time 25°C to peak temperature:	480 sec. max.



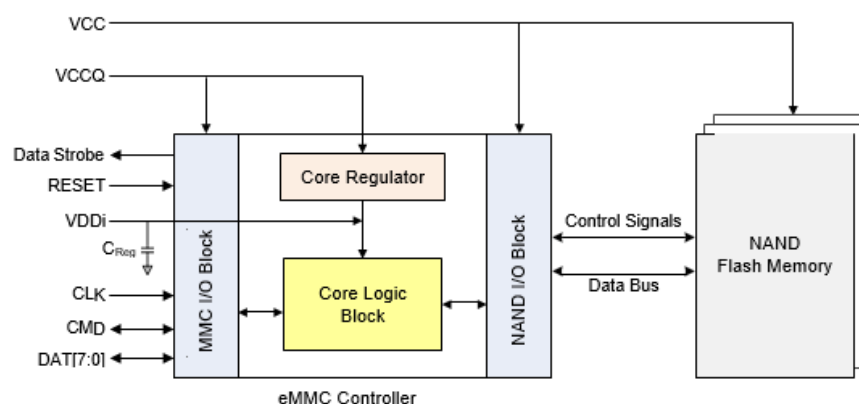
6 ELECTRICAL SPECIFICATION

6.1 Electrical Interface

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device; V_{CCQ} is used for the controller and the eMMC interface voltage.

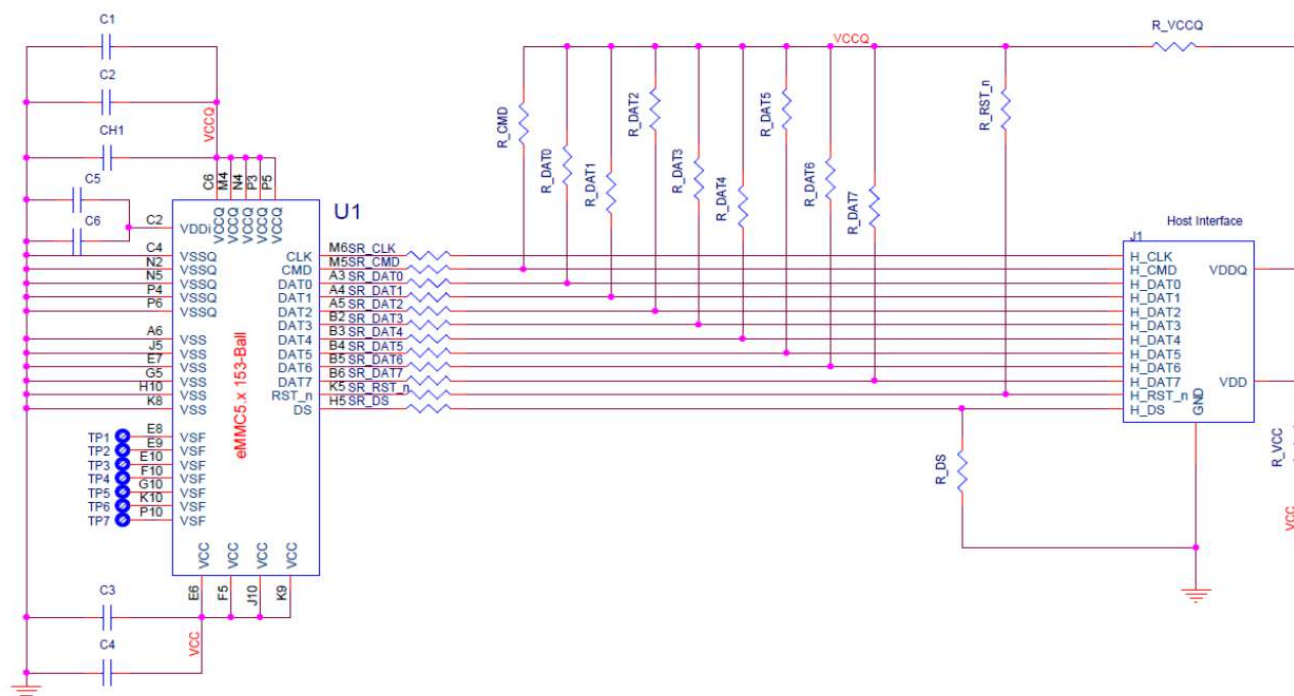
Figure 4: System Architecture



6.2 DC Specifications

Table 7: Power Requirements

Symbol	Parameter	Value (Minimum)	Value (Typical)	Value (Maximum)	Unit
V_{CC}	Voltage supply to Flash memory	2.7	3.3	3.6	V
V_{CCQ}	Voltage supply to host interface	2.7 (high range) 1.70 (low range)	3.3 (high range) 1.80 (low range)	3.6 (high range) 1.95 (low range)	V
V_{DDi}	Internal voltage regulator connection to external capacitor	-	-	-	-

Figure 5: Recommended eMMC Connection


Note:

- 1) Connect coupling capacitors with VCC/VCCQ and VSS as close as possible.
- 2) Separate the VCC and VCCQ power.
- 3) Lay the VSS between the CLK and the Data lines.

6.3 Capacitor and Resistor Specifications

Table 8: Capacitor and Resistor Specifications

Parameter ¹	Symbol	Min.	Max.	Recommended	Unit	Remark
Pull-up resistance for CMD	R_CMD	4.7	50	10	kΩ	To prevent bus from floating
Pull-up resistance for DAT0-7	R_DAT0~7	10	50	10	kΩ	To prevent bus from floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	10	kΩ	It's not necessary to put pull-up resistance on RST_n (H/W reset) line if host does not use H/W reset.
Pull-down resistance for R_DS	R_DS	10	50	10	kΩ	
Impedance on CLK/CMD/DAT0~7	-	45	55	50	Ω	Impedance match

Parameter ¹	Symbol	Min.	Max.	Recommended	Unit	Remark
Serial resistance on CLK	SR_CLK	-	-	0	Ω	To put serial resistance except 0 ohm, check timing are all in Spec.
Serial resistance on power trace	R_VCC R_VCCQ	-	-	0	Ω	Typical size 0603 or 0805.
Serial resistance on CMD/DS/DAT0~7/RS T_n	SR_CMD SR_DS SR_DAT0~7 SR_RST_n	-	-	0	Ω	To put serial resistance except 0 ohm, check timing are all in Spec.
VccQ capacitor value	C1	2.2	4.7	4.7	μF	Coupling capacitor should be connected with VccQ and VssQ as closely as possible.
	C2	0.1	0.22	0.1		
	C _{H1}	1	2.2	1	μF	CH1 should be placed adjacent to VCCQ-VSSQ balls. It should be located as close as possible to the balls defined in order to minimize connection parasitic.
Vcc capacitor value	C3	2.2	4.7	4.7	μF	Coupling capacitor should be connected with Vcc and Vss as closely as possible.
	C4	0.1	0.22	0.22		
VDDi capacitor value(C _{REG})	C5	1	4.7	2.2	μF	Coupling capacitor should be connected with VDDi and Vss as closely as possible.
	C6	0.1	0.22	0.1		
Vendor Specific	TP1 – TP7	-	-	-	-	This function of these signal is defined and specified by the controller vendor. A pin that is not be used in normal applications and that may or may not have an internal connection. The VSF signals shall be treated as NU signals by the user. The VSF signals shall reserved test pints on the PCB, avoid reference highspeed layer and power plane.

¹ It doesn't matter to put Pull-up resistors and Serial resistors closer to host or eMMC. However, it's recommended to put all resistors on the same PCB side (Top or Bottom).

7 REGISTER

The registers used in the SMART eMMC are shown in the table below. These registers are described in the sections that follow:

Table 9: Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

7.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 10: CID Register Field Parameters

Name	Field	Width (Bits)	CID Bits	SMART CID Value	
Manufacturer ID	MID	8	[127:120]	0xF6	
Reserved	-	6	[119:114]	--	
Device / BGA	CBX	2	[113:112]	0x01	
OEM/application ID	OID	8	[111:104]	0x00	
Product name	PNM ⁽¹⁾	48	[103:56]	8GB	8GP1CΔ (0x38 0x47 0x50 0x31 0x43 0x20)
				16GB	AGP1CΔ (0x41 0x47 0x50 0x31 0x43 0x20)
				32GB	BGP1CΔ (0x42 0x47 0x50 0x31 0x43 0x20)
Product revision	PRV	8	[55:48]	0x10	
Product serial number	PSN	32	[47:16]	-- ⁽²⁾	
Manufacturing date	MDT	8	[15:8]	-- ⁽³⁾	
CRC7 checksum	CRC	7	[7:1]	-- ⁽⁴⁾	
reserved	-	1	0	0x01	

(1) The product name uses ASCII code and 'Δ' is a space (0x20).

(2) Unique for each device. 32-bit unsigned binary integer.

(3) 2 hex digits for device manufacturing month and year.

(4) CRC for CID register. Different for each device.

7.2 OCR Register

The card identification (OCR) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 11: OCR Register Field Definitions

V _{DD} Voltage Window	Width (Bits)	OCR Bits	OCR Value
Ready/Busy	1	[31]	card power up status bit (busy) ⁽¹⁾
Access Mode	2	[30:29]	10b
Reserved	5	[28:24]	--
2.7-3.6V	9	[23:15]	1 1111 1111b
2.0-2.6V	7	[14:8]	000 0000b
1.70-1.95V	1	[7]	1b
Reserved	7	[6:0]	--

(1) This bit is set to low if the device has not finished the power up routine.

7.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 12: CSD Register Field Parameters

Name	Field	Width (Bits)	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	[127:126]	0x03
System specification version	SPEC_VERS	4	[125:122]	0x04
Reserved	-	2	[121:120]	--
Data read access time 1	TAAC	8	[119:112]	0x4F
Data read access time 2 in CLK cycles (NSAC x 100)	NSAC	8	[111:104]	0x01
Maximum bus clock frequency	TRAN_SPEED	8	[103:96]	0x32

Name	Field	Width (Bits)	CSD Bits	CSD Value
Device command classes	CCC	12	[95:84]	0xF5
Maximum read data block length	READ_BL_LEN	4	[83:80]	0x09
Partial blocks for reads supported	READ_BL_PARTIAL	1	[79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0x0
DSR implemented	DSR_IMP	1	[76]	0x0
Reserved	-	2	[75:74]	--
Device size	C-SIZE	12	[73:62]	0xFFFF
Maximum read current as VDD,min	VDD_R_CURR_MIN	3	[61:59]	0x7
Maximum read current as VDD,max	VDD_R_CURR_MAX	3	[58:56]	0x7
Maximum write current as VDD,min	VDD_W_CURR_MIN	3	[55:53]	0x7
Maximum write current as VDD,max	VDD_W_CURR_MAX	3	[52:50]	0x7
Device size multiplier	C-SIZE_MULT	3	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	[31]	0x1
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0x0
Write-speed factor	R2W_FACTOR	3	[28:26]	0x2
Maximum write data block length	WRITE_BL_LEN	4	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0x0
Reserved	-	4	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	[16]	0x0
File-format group	FILE_FORMAT_GRP	1	[15]	0x0
Copy flag (OTP)	COPY	1	[14]	0x0
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0x0
Temporary write protection	TEMP_WRITE_PROTECT	1	[12]	0x0
File format	FILE_FORMAT	2	[11:10]	0x0
ECC code	ECC	2	[9:8]	0x0
CRC	CRC	7	[7:1]	0x30

Name	Field	Width (Bits)	CSD Bits	CSD Value
Not used; always 1	-	1	[0]	0x1

7.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 13: ECSD Register Field Parameters

Name	Field		Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Reserved	-		6	-	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR		1	R	[505]	0x00
Supported command sets	S_CMD_SET		1	R	[504]	0x01
HPI features	HPI_FEATURES		1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT		1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS		1	R	[501]	0x3C
Max packed write commands	MAX_PACKED_WRITES		1	R	[500]	0x3C
Data tag support	DATA_TAG_SUPPORT		1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE		1	R	[498]	0x03
Tag resources size	TAG_RES_SIZE		1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES		1	R	[496]	0x05
Large unit size	LARGE_UNIT_SIZE_M1	8GB	1	R	[495]	0x07
		16GB				0x0F
		32GB				0x0F
Extended partitions attribute support	EXT_SUPPORT		1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES		1	R	[493]	0x01

Name	Field	Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	65535
Reserved	-	177	-	[486:306]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	-
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	Variable
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	Variable
Pre EOL information	PRE_EOL_INFO	1	R	[267]	Variable
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x01
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device version	Device version	2	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	Variable
Power class for 200MHz DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	1024
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x19
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0xFF
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x64
Reserved	-	1	-	[240]	--
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00

Name	Field		Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195		1	R	[238]	0x00
Power class for 200 MHz at 1.95V, VCC = 3.6V	PWR_CL_200_195		1	R	[237]	0x00
Power class for 200 MHz at 1.3V, VCC = 3.6V	PWR_CL_200_130		1	R	[236]	0x00
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52		1	R	[235]	0x00
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52		1	R	[234]	0x00
Reserved	-		1	-	[233]	--
TRIM multiplier	TRIM_MULT	8GB	1	R	[232]	0x11
		16GB				0x11
		32GB				0x22
Secure feature support	SEC_FEATURE_SUPPORT		1	R	[231]	0x55
SECURE ERASE multiplier	SEC_ERASE_MULT	8GB	1	R	[230]	0x25
		16GB				0x2C
		32GB				0x21
SECURE TRIM multiplier	SEC_TRIM_MULT	8GB	1	R	[229]	0x25
		16GB				0x2C
		32GB				0x21
Boot information	BOOT_INFO		1	R	[228]	0x07
Reserved	-		1	-	[227]	--
Boot partition size	BOOT_SIZE_MULT		1	R	[226]	0x20
Access size	ACC_SIZE	8GB	1	R	[225]	0x07
		16GB				0x08
		32GB				0x09
High-capacity erase unit size	HC_ERASE_GRP_SIZE		1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	8GB	1	R	[223]	0x11
		16GB				0x11
		32GB				0x22

Name	Field	Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Reliable write-sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (V _{CC})	S_C_VCC	1	R	[220]	0x0A
Sleep current (V _{CCQ})	S_C_VCCQ	1	R	[219]	0x0B
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x14
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x13
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x0F
Sector count	SEC-COUNT	8GB	4	[215:212]	15433728
		16GB			30932992
		32GB			61865984
Reserved	-	1	-	[211]	--
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x08
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x08
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x08
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x08
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x08
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x08
Reserved	-	1	-	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00

Name	Field	Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x03
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x04
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card type	CARD_TYPE	1	R	[196]	0x57
Reserved	-	1	-	[195]	--
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	-	1	-	[193]	--
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x07
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	-	1	-	[190]	--
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	-	1	-	[188]	--
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	-	1	-	[186]	--
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x01
Reserved	-	1	-	[184]	--
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x02
Reserved	-	1	-	[182]	--
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved	-	1	-	[180]	--
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved	-	1	-	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x00

Name	Field		Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Boot write protection status registers	BOOT_WP_STATUS		1	R	[174]	0x00
Boot area write protection register	BOOT_WP		1	R/W, R/W/C_P	[173]	0x00
Reserved	-		1	-	[172]	--
User write protection register	USER_WP		1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	-		1	-	[170]	--
Firmware configuration	FW_CONFIG		1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT		1	R	[168]	0x20
Write reliability setting register	WR_REL_SET		1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM		1	R	[166]	0x04
Start sanitize operation	SANITIZE_START		1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START		1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN		1	R/W	[163]	0x00
Hardware reset function	RST_n_FUNCTION		1	R/W	[162]	0x00
HPI management	HPI_MGMT		1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT		1	R	[160]	0x07
Maximum enhanced area size	MAX_ENH_SIZE_MULT	8GB	3	R	[159:157]	471
		16GB				944
		32GB				1888
Partitions attribute	PARTITIONS_ATTRIBUTE		1	R/W	[156]	0x00
Partitioning setting	PARTITIONING_SETTING-COMPLETED		1	R/W	[155]	0x00
General-purpose partition size	GP_SIZE_MULT		12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT		3	R/W	[142:140]	0x00

Name	Field	Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved	-	1	-	[135]	--
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved	-	2	-	[129:128]	--
Vendor specific fields	VENDOR_SPECIFIC_NFIELD	64	<vs>	[127:64]	-
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 command control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	0x00

Name	Field		Size (Bytes)	Cell Type ⁽¹⁾	ECSD Bytes	ECSD Values
Flushing of the cache	FLUSH_CACHE		1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL		1	R/W	[31]	0x00
Mode config	MODE_CONFIG		1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES		1	W/E_P	[29]	0x00
Reserved	-		2	-	[28:27]	--
FFU status	FFU_STATUS		1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE		4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	8GB	4	R	[21:18]	7651328
		16GB				15335424
		32GB				30670848
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT		1	R/W/E & R	[17]	0x01
Secure removal type	SECURE_REMOVAL_TYPE		1	R/W & R	[16]	0x01
Reserved	-		16	-	[15:0]	--

Notes:

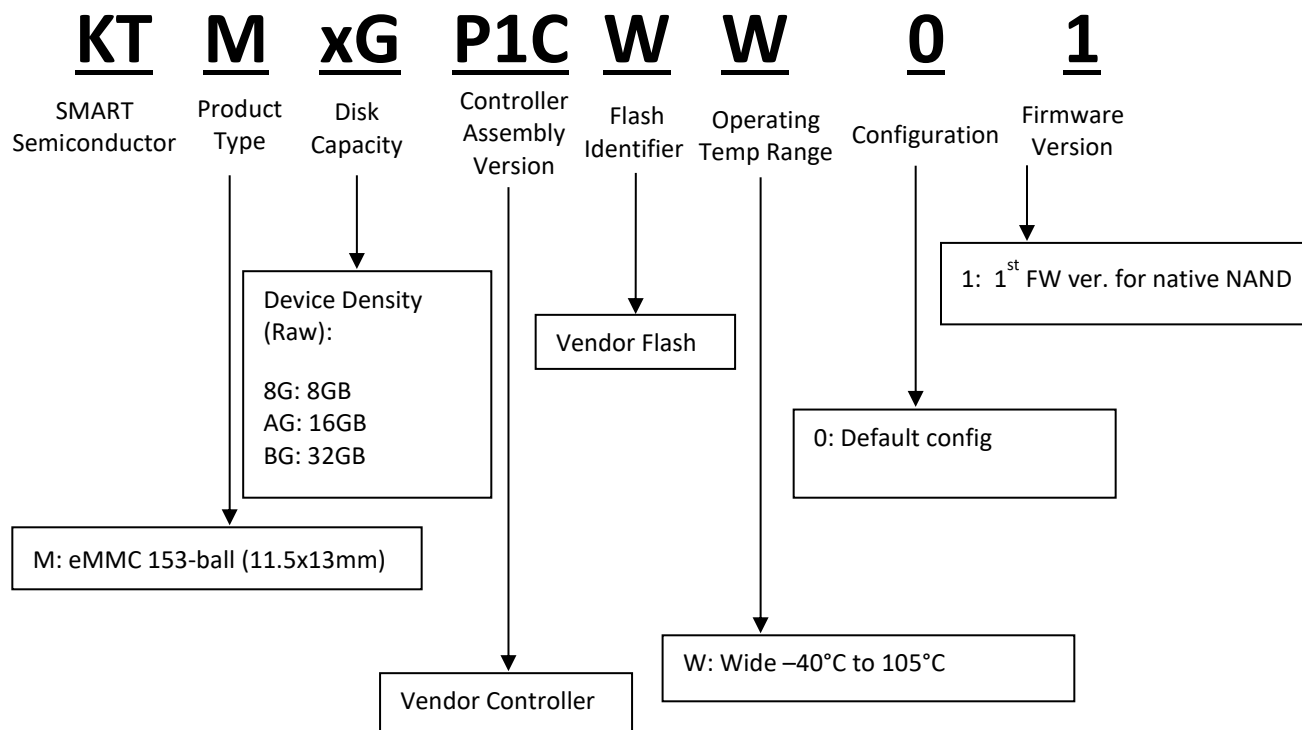
- The definitions of cell type are shown as follows:
R: Read only.
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable. R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable. W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.
- Reserved bits should be read as "0".
- The column marked with "-" is undefined.

8 PART NUMBERS

Table 14: Part Numbering Information

Capacity	Part Number
8GB	KTM8GP1CWW01
16GB	KTMAGP1CWW01
32GB	KTMBGP1CWW01

8.1 Part Number Decoder



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