

## Reliability Summary Report

Product Type: 4Gb (256Mx16) DDR3

\_\_\_\_\_ 4Gb (512Mx8) DDR3

Part Number: KTDM4G3C618BGCEA

KTDM4G3C618BGIEA

KTDM4G3C818BGCEA

\_\_\_\_\_ KTDM4G3C818BGIEA

Package: 96 ball BGA

\_\_\_\_\_ 78 ball BGA

## 1. Features

- SSTL\_15:VDD/VDDQ = 1.5V( $\pm 0.075$ V)
- SSTL\_135:VDD/VDDQ = 1.35V(-0.067V/+0.1V)
- 8n Prefetch Architecture
- Differential Clock (CK, /CK) and Data Strobe (DQS, /DQS)
- Double-data rate on DQs, DQS and DM
- Auto Refresh and Self Refresh Modes
- Partial Array Self Refresh (PASR)
- Power Down Mode
- Configurable DS for system compatibility
- Configurable On-Die Termination
- ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm  $\pm 1\%$ )
- Write Leveling via MR settings
- Read Leveling via MPR
- CAS Latency (5/6/7/8/9/10/11/12)
- CAS Write Latency (5/6/7/8/9/10/11/12)
- Additive Latency (0/CL-1/CL-2)
- Write Recovery Time (5/6/7/8/10/12/14/16)
- Burst Type (Sequential/Interleaved)
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Self Refresh Temperature Range (Normal/Extended)
- Output Driver Impedance (34/40)
- On-die Termination of Rtt\_Nom (20/30/40/60/120)
- On-die Termination of Rtt\_WR (60/120)
- Precharge Power Down (slow/fast)

## 2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM4G3C618BGCEA	1.35V/1.5V	DDR3L-1866 (13-13-13)	96 ball BGA	Commercial	Pb-free
KTDM4G3C618BGIEA	1.35V/1.5V	DDR3L-1866 (13-13-13)	96 ball BGA	Industrial	Pb-free
KTDM4G3C818BGCEA	1.35V/1.5V	DDR3L-1866 (13-13-13)	78 ball BGA	Commercial	Pb-free
KTDM4G3C818BGIEA	1.35V/1.5V	DDR3L-1866 (13-13-13)	78 ball BGA	Industrial	Pb-free

**Note:**

The above description is extracted from the datasheet. Please refer to the document for detailed information.

### 3. Product Qualification – Die Related Tests

#### 3.1. Test Conditions & Criteria – Die Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	High Temperature Operating Life Test	Ta=125°C V>=1.1Vcc Dynamic	105	LTPD*1=5%
2	High Temperature Static Life	Ta=125°C V>=1.1Vcc Static	77	LTPD=5%
3	High Temperature Bake Test	Ta=150°C	77	LTPD=5%
4	ESD	HBM MM CDM	3/case	>±2KV >±200V >±1KV
5	Latch-Up	Vtrig	3/case	>Vcc+0.5Vcc <Vss-0.5Vcc
		Itrig	3/case	>±100mA

Note \*1: LTPD (MIL-S-19500C) → Lot Tolerance Percent Defective

-- A single lot sampling concept that statistically ensures rejection of 90% of all lots having a greater % defective than the specified LTPD

#### 3.2. Test Result – Die Related Tests

No.	Item	Condition	Sample Size	Results (Cumulative Failure)			Comment
				168hrs	500hrs	1000hrs	
1	High Temperature Operating Life Test	Ta=125°C V>=1.1Vcc Dynamic	105	168hrs	500hrs	1000hrs	Pass
				0f/105	0f/105	0f/105	
2	High Temperature Static Life	Ta=125°C V>=1.1Vcc Static	77	0f/77	0f/77	0f/77	Pass
3	High Temperature Bake Test	Ta=150°C	77	-	0f/77	0f/77	Pass
4	ESD	HBM MM CDM	3/case	>±2KV >±200V >±1KV	-	-	Pass
5	Latch-Up	Vtrig	3/case	>2.37V <-1.5V	-	-	Pass
		Itrig		>±200mA			

## 4. Product Qualification, Plastic Package Related Tests

### 4.1. Test Conditions & Criteria – Plastic Package Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	Moisture Re-flow Sensitivity	T/C x 5cyc ↓ Bake x 24hrs ↓ Moisture soaking (JEDEC level III) ↓ IR(260°C) Reflow x3	238	LTPD=7%
2*	Pressure Cooker Test (Autoclave)	Ta=121°C RH=100% 29.7 Psia	55	LTPD=7%
3*	Highly Accelerated Temperature and Humidity Stress Test	Ta=130°C RH=85% Vcc=1.1Vcc 33.3 Psia	32	LTPD=7%
4*	Temperature Cycle Test	-55°C (10min) ↑↓ 125°C (10min) AIR	55	LTPD=7%
5*	Thermal Shock Test	-55°C (10min) ↑↓ 125°C (10min) LIQUID	55	LTPD=7%

\*Samples are sourced from pre-conditioned process (Bake x 24hr → Moisture soaking (JEDEC level III) → IR Reflow x3)

## 4.2. Test Conditions & Results – Environment Tests (BGA96)

No.	Item	Condition	Sample Size	Results (Cumulative Failure)	Comment
1	Moisture Re-flow Sensitivity (MRS)	T/C x 5cyc ↓ Bake 125°C x 24hrs ↓ Soaking 30°C / RH 60% x192hrs ↓ IR(260°C) Reflow x3	238	0f/238	Pass
2	Pressure Cooker Test (PCT)	Ta=121°C RH=100% 29.7 Psia	55	168hrs	Pass
				0f/55	
3	Highly Accelerated Temperature and Humidity Stress Test (HAST)	Ta=130°C RH=85% Vcc=1.1Vcc 33.3 Psia	32	100hrs	Pass
				0f/32	
4	Temperature Cycle Test (TC)	-55°C (10min) ↑↓ 125°C (10min) AIR	55	500cyc	Pass
				0f/55	
5	Thermal Shock Test (TS)	-55°C (10min) ↑↓ 125°C (10min) LIQUID	55	500cyc	Pass
				0f/55	

Note: Item 2-5 used samples after MRS flow.

### 4.3. Test Conditions & Results – Environment Tests (BGA78)

No.	Item	Condition	Sample Size	Results (Cumulative Failure)	Comment
1	Moisture Re-flow Sensitivity (MRS)	T/C x 5cyc ↓ Bake 125°C x 24hrs ↓ Soaking 30°C / RH 60% x192hrs ↓ IR(260°C) Reflow x3	238	0f/238	Pass
2	Pressure Cooker Test (PCT)	Ta=121°C RH=100% 29.7 Psia	55	168hrs	Pass
				0f/55	
3	Highly Accelerated Temperature and Humidity Stress Test (HAST)	Ta=130°C RH=85% Vcc=1.1Vcc 33.3 Psia	32	100hrs	Pass
				0f/32	
4	Temperature Cycle Test (TC)	-55°C (10min) ↑↓ 125°C (10min) AIR	55	500cyc	Pass
				0f/55	
5	Thermal Shock Test (TS)	-55°C (10min) ↑↓ 125°C (10min) LIQUID	55	500cyc	Pass
				0f/55	

Note: Item 2-5 used samples after MRS flow.

## 5. ESD Test Data

### 5.1. Human Body Model (Method: EIA/JESD22-A114)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			Min (for 3ea)	Max (for 3ea)	
R=1.5KΩ  C=100pF	Pin to Vcc (+)	3	> 6000V	> 6000V	
	Pin to Vcc (-)	3	> 4500V	> 6000V	
	Pin to Vss (+)	3	> 5500V	> 6000V	
	Pin to Vss (-)	3	> 6000V	> 6000V	
	Pin to Pin (+)	3	> 6000V	> 6000V	
	Pin to Pin (-)	3	> 6000V	> 6000V	
	Vcc to Vss (+)	3	> 6000V	> 6000V	
	Vcc to Vss (-)	3	> 6000V	> 6000V	

### 5.2. Machine Model (Method: EIA/JESD22-A115)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			Min (for 3ea)	Max (for 3ea)	
R=0Ω  C=200pF	Pin to Vcc (+)	3	> 350V	> 500V	
	Pin to Vcc (-)	3	> 200V	> 500V	
	Pin to Vss (+)	3	> 350V	> 500V	
	Pin to Vss (-)	3	> 350V	> 450V	
	Pin to Pin (+)	3	> 350V	> 500V	
	Pin to Pin (-)	3	> 300V	> 500V	
	Vcc to Vss (+)	3	> 400V	> 450V	
	Vcc to Vss (-)	3	> 400V	> 450V	

### 5.3. Non-Socket Charged Device Model (JESD22-C101)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			Min (for 3ea)	Max (for 3ea)	
Non-Socket CDM	±1000V	3	FT Pass	FT Pass	



## 6. Latch-Up Test Data: for JEDEC-STD-78

Trigger Mode	Test Pin	Sample Size	Latch-Up Triggering Range	
			Min (for 3ea)	Max (for 3ea)
+VT*	I/P	3	3.0V	3.0V
	I/O		3.0V	3.0V
-VT*	I/P	3	1.5V	1.5V
	I/O		1.5V	1.5V
+IT*	I/P	3	300mA	300mA
	I/O		300mA	300mA
-IT*	I/P	3	300mA	300mA
	I/O		300mA	300mA
Power Transient* (Vcc-Vss)	-	3	3.0V	3.0V

\*Latch-up did not occur

## 7. Estimation of Long-term Failure Rate

### 7.1. Model

$$L = A \exp(EA/kT) * \exp(-BV_{cc})$$

Where:

L: Life time

Ea: Activation energy

B: Voltage acceleration factor

T: Absolute temperature

Vcc: Applied voltage

### 7.2. Statistical Analysis

$$\lambda_{\max} = \frac{\chi^2(1-\alpha)}{2t} \quad [\text{with } df=2(r+1)]$$

$$MTBF_{\min} = 1/\lambda_{\max}$$

Where:

$\lambda_{\max}$  = Maximum or worst-case failure rate

MTBF<sub>min</sub> = Minimum (worst-case) expected MTBF

$\chi^2$  = Chi square distribution

r = Number of failures

df = Degrees of freedom

t = total number of test hours (number of devices x number of hours)

$\alpha$  = Statistical error expected in estimate. For 60% confidence,  $\alpha = 0.4$  or  $1-\alpha = 0.6$

### 7.3. Calculation of HTOL Data

Acceleration Factor:  $E_a = 0.5\text{eV}$ ,  $B = 7.0 (1/V)$

Field Condition:  $T_a = 55^\circ\text{C}$ ,  $V_{cc} = 1.5\text{V}$

HTOL (Condition)

Acceleration:  $A_T(125^\circ\text{C}:55^\circ\text{C}) = 22.45$  times

$V_{cc}(1.8\text{V}:1.5\text{V}) \leftrightarrow V_{\text{internal}}(3.4\text{V}:2.8\text{V})$

$A_v(3.4\text{V}:2.8\text{V}) = 66.69$  times

$$\text{Estimated failure rate} = \frac{1.83 \times 10^9}{2 \times (105 \times 1000) \times 22.45 \times 66.69}$$

$$= 5.83 \text{ FIT}$$

## 8. Continuous Quality Study Data

### 8.1. High Temperature Operating Life Test (HTOL)

125°C, 1000 hrs, Dynamic, Stress Vcc (shown in Remark)

Time Period	FAB Site	Reject/Devices	Failure Rate (FIT)	Reject Information	Remark
Q2 2021	PSC	0f/105	13.4	NA	Vcc = 1.8V
Q3 2021	PSC	0f/105	13.4	NA	Vcc = 1.8V
Q4 2021	PSC	0f/105	13.4	NA	Vcc = 1.8V

### 8.2. High Temperature Bake (HTB)

150°C, No Bias, 1000 hrs

Time Period	FAB Site	Package Type	Reject/Devices	Cumulative % Fail	Remark
Q2 2021	PSC	BGA 96	0f/77	0%	NA
Q3 2021	PSC	BGA 96	0f/77	0%	NA
Q4 2021	PSC	BGA 96	0f/77	0%	NA

### 8.3. High Temperature Static Life Test (HTSL)

125°C, 1000 hrs, Static, Stress Vcc (shown in Remark)

Time Period	FAB Site	Package Type	Reject/Devices	Cumulative % Fail	Remark
Q2 2021	PSC	BGA 96	0f/45	0%	Vcc = 1.8V
Q3 2021	PSC	BGA 96	0f/45	0%	Vcc = 1.8V
Q4 2021	PSC	BGA 96	0f/45	0%	Vcc = 1.8V

### 8.4. Moisture / Reflow Sensitivity (Simulated SMT Process, MRS)

TC (-55°C ~ 125°C), Baking 125°C x 24 hrs, 30°C, 60% RH, 192 hrs, IR Reflow (Max: 260°C), 3 Passes

Time Period	Package Type	Reject/Devices	Cumulative % Fail	Reject Information
Q2 2021	BGA 96	0f/149	0%	NA
Q3 2021	BGA 96	0f/149	0%	NA
Q4 2021	BGA 96	0f/149	0%	NA

## 8.5. Pressure Cooker Test (Autoclave, AC)

121°C, 100% RH, 29.7 psia, 168 hrs

Time Period	Package Type	Reject/Devices	Cumulative % Fail	Reject Information
Q2 2021	BGA 96	0f/55	0%	NA
Q3 2021	BGA 96	0f/55	0%	NA
Q4 2021	BGA 96	0f/55	0%	NA

## 8.6. Highly Accelerated Stress Test

130°C, 85% RH, 33.3 psia, 1.65V, 100 hrs

Time Period	Package Type	Reject/Devices	Cumulative % Fail	Reject Information
Q2 2021	BGA 96	0f/32	0%	NA
Q3 2021	BGA 96	0f/32	0%	NA
Q4 2021	BGA 96	0f/32	0%	NA

## 8.7. Temperature Cycle

-55°C to 125°C, Air to Air, 500 cycles

Time Period	Package Type	Reject/Devices	Cumulative % Fail	Reject Information
Q2 2021	BGA 96	0f/55	0%	NA
Q3 2021	BGA 96	0f/55	0%	NA
Q4 2021	BGA 96	0f/55	0%	NA