Reliability Summary Report

Product Type:	8Gb (512Mx16) DDR4
	8Gb (1Gx8) DDR4
Part Number:	KTDM8G4B632BGCBC
	KTDM8G4B632BGIBC
	KTDM8G4B832BGCBC
	KTDM8G4B832BGIBC
Package:	96 ball BGA
	78 ball BGA

1. Features

- Power supply (JEDEC standard 1.2V)
  - VDD = 1.2V ± 5%
  - VPP = 2.375V to 2.75V
- 16 internal banks – 16 banks (4 banks x 4 bank groups) for x8 product
- 8 internal banks - 8 banks (4 banks x 2 bank groups) for x 16 product
- Interface: Pseudo Open Drain (POD)
- Burst Length (BL): 8 and 4 with Burst Chop (BC)
- CAS Latency (CL): 10,(11),12,(13),14,(15),16,(17),18,19,20,22,24
- CAS Write Latency (CWL): 9,10,11,12,14,16,18,20
- On-Die Termination (ODT): nom. values of RZQ/7, RZQ/5 (RZQ = 240Ω)
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  Average refresh period
  - 7.8µs at 0°C ≤ TC ≤ +85°C or -40°C ≤ TC ≤ +85°C
  - 3.9µs at +85°C < TC ≤ +95°C
- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS_t and DQS_c) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Write Cyclic Redundancy Code (CRC) for DQ error detect and inform it to controller during high-speed operation

- Data Bus Inversion (DBI)
  - Improve the power consumption and signal integrity of the memory interface (x16 product only)
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity for command/address signal error detect and inform it to controller
- VREFDQ training
  - VREFDQ generate inside DRAM and further train per DRAM
- Per DRAM Addressability (PDA)
  - Each DRAM can be set a different mode register value individually and has individual adjustment.
- Fine granularity refresh
  - 2x, 4x mode for smaller tRFC
- Programmable Partial Array Self-Refresh (PASR)
- RESET_n pin for power-up sequence and reset function
- Operating case temperature range:
  - Commercial: T_C = 0°C to +95°C
  - Industrial: T_C = -40°C to +95°C

2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM8G4B632BGCBC	1.2V	DDR4-3200 (22-22-22)	96 ball BGA	Commercial	Pb-free
KTDM8G4B632BGIBC	1.2V	DDR4-3200 (22-22-22)	96 ball BGA	Industrial	Pb-free
KTDM8G4B832BGCBC	1.2V	DDR4-3200 (22-22-22)	78 ball BGA	Commercial	Pb-free
KTDM8G4B832BGIBC	1.2V	DDR4-3200 (22-22-22)	78 ball BGA	Industrial	Pb-free

Note:

The above description is extracted from the datasheet. Please refer to the document for detailed information.

3. Product Qualification – Die Related Tests

3.1. Test Conditions & Criteria – Die Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	High Temperature Operating Life Test	Ta=125°C V>=1.1VDD	76	0A/1R
2	Low Temperature Operating Life Test	Ta=-25°C V>=1.1VDD	76	0A/1R
3	High Temperature Bake Test	Ta=150°C	76	0A/1R
4	ESD	HBM CDM	40 30	>±1KV >±500V
5	Latch-Up	Vtrig	10	>VDD+0.5VDD <Vss-0.5VDD
		Itrig	40	>±100mA

3.2. Test Result – Die Related Tests

No.	Item	Condition	Sample Size	Results (Cumulative Failure)			Comment
1	High Temperature Operating Life Test	Ta=125°C V>=1.1VDD	76	168hrs 0f/76	300hrs 0f/76	1000hrs -	
2	Low Temperature Operating Life Test	Ta=-25°C V>=1.1VDD	76	0f/76	0f/76	-	
3	High Temperature Bake Test (HTB)	Ta=150°C	76	0f/76	0f/76	0f/76	
4	ESD	HBM CDM	40 30	>±2KV >±1KV	-	-	Pass
5	Latch-Up	Vtrig	10	>1.8V <-0.6V	-	-	Pass
		Itrig	40	>±200mA			

4. Product Qualification, Plastic Package Related Tests

4.1. Test Conditions & Criteria – Plastic Package Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	Moisture Re-flow Sensitivity	T/C x 5cyc ↓ Bake x 24hrs ↓ Moisture soaking (JEDEC level III) ↓ IR(260˚C) Reflow x3	33	0A/1R
2*	Highly Accelerated Temperature and Humidity Stress Test	Ta=130˚C RH=85% VDD=1.1VDD 33.3 Psia	73	0A/1R
3*	Temperature Cycle Test	-55˚C (10min) ↑↓ 125˚C (10min) AIR	76	0A/1R

*Samples are sourced from pre-conditioned process (Bake x 24hr → Moisture soaking (JEDEC level III) → IR Reflow x3)

4.2. Test Conditions & Results – Environment Tests (BGA96)

No.	Item	Condition	Sample Size	Results (Cumulative Failure)	Comment
1	Moisture Re-flow Sensitivity (MRS)	T/C x 5cyc ↓ Bake 125°C x 24hrs ↓ Soaking 30°C / RH 60% x192hrs ↓ IR(260°C) Reflow x3	33	Pass	
2	Highly Accelerated Temperature and Humidity Stress Test (HAST)	Ta=130°C RH=85% VDD=1.1VDD 33.3 Psia	116	168hrs Pass	
3	Temperature Cycle Test (TC)	-55°C (10min) ↑↓ 125°C (10min) AIR	116	600cyc Pass	

4.3. Test Conditions & Results – Environment Tests (BGA78)

No.	Item	Condition	Sample Size	Results (Cumulative Failure)	Comment
1	Moisture Re-flow Sensitivity (MRS)	T/C x 5cyc ↓ Bake 125°C x 24hrs ↓ Soaking 30°C / RH 60% x192hrs ↓ IR(260°C) Reflow x3	33	Pass	
2	Highly Accelerated Temperature and Humidity Stress Test (HAST)	Ta=130°C RH=85% VDD=1.1VDD 33.3 Psia	76	168hrs Pass	
3	Temperature Cycle Test (TC)	-55°C (10min) ↑↓ 125°C (10min) AIR	76	1000cyc Pass	

5. ESD Test Data

5.1. Human Body Model (Method: EIA/JESD22-A114)

Test Condition	Test Mode	Sample Size	Test Results	Remark
Room Temperature	±1000V	40	Pass	

5.2. Non-Socket Charged Device Model (JESD22-C101)

Test Condition	Test Mode	Sample Size	Test Results	Remark
Non-Socket CDM	±500V	30	Pass	

6. Latch-Up Test Data: for JEDEC-STD-78

Lach-Up Test	Test Mode	Sample Size	Test Result
V-test	6V	10	Pass
I-Test	150mA	40	Pass