# SMARTsemi
# Memory IC Datasheet

## Industrial Grade eMMC 153b

*July 2022*
*Rev 0.1*

# REVISION HISTORY

| Date | Revision | Section(s) | Description |
|---|---|---|---|
| July 2022 | 0.1 | All | Initial Release |

**ESD Caution – Handling**
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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# 1 GENERAL DESCRIPTION

## 1.1 Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, Global wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMARTsemi's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

## 1.2 Features

- Industrial Standard Interface
  - JEDEC / eMMC Standard Version 5.1 Compliant

- eMMC 5.1 Enhanced Features
  - 11-signal interface (including CMD, CLK, DAT[7:0], and RST_n)
  - Programmable bus width: 1-bit, 4-bit, and 8-bit
  - Supports HS400 high speed interface timing mode
  - Up to 200MHz clock frequency
  - Supports eMMC Field firmware update (FFU)
  - Supports eMMC production state awareness (PSA)
  - Supports eMMC device health report
  - High-speed, Dual Data Rate Boot support
  - Supports Boot and Alternative Boot Mode
  - Replay Protected Memory Block (RPMB)
  - Trim, Sanitize, Discard, Secure Erase
  - High Priority Interrupt (HPI)
  - Background Operations, Garbage Collection and WearLeveling
  - Reliable Write
  - Supports Command Queuing
  - Supports Enhanced Strobe in HS400 Mode
  - Supports eMMC Background Operation Control
  - Supports Lock/Unlock
  - Supports Secure Removal Type
  - Supports Configurable Drive Strength
  - Supports Write protect, Secure Write Protection
  - Supports Cache, Cache Barrier, Cache Flushing Report
  - Hardware/ Software Reset
  - Supports PON, Sleep/Awake

- Robust Data Protection and Endurance
  - Configurable ECC engine with zero overhead pipeline greatly reduces data loss rates and increases data endurance
  - Static data refresh and early block failure monitoring/retirement ensure the data reliability
  - Power loss detection and mapping table auto-rebuild algorithm support power-down data protection
  - Global wear leveling maximizes product lifespan with minimal wear leveling and write amplification overhead

- Supply Voltage
  - eMMC Interface Power (VCCQ): 1.70-1.95V

  - eMMC Interface Power (VCCQ): 2.7-3.6V[1]
  - NAND Memory Power (VCC): 2.7-3.6V

- Dynamic power management technology enables multiple power saving modes

- Multiple Densities and Packages
  - Available in 4GB MLC mode density
  - 153-ball standard BGA packages
  - Green Package, REACH and RoHS Compliant

- Operating Temperature
  - Industrial Grade: -40°C ~ +85°C

Note: [1] HS200 and HS400 mode are not supported when VCCQ is in 2.7-3.6V.

# 2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

## 2.1 Performance

**Table 1: Performance Table**

**MLC Partition Performance**

| Capacity | HS400 Performance MLC MODE | | | |
|---|---|---|---|---|
| | Seq. Read (MB/s) | Seq. Write (MB/s) | Random Read 4KB (IOPS) | Random Write 4KB (IOPS) |
| 4 GB (native) No pre-configuration | 170 | 10 | 5345 | 980 |

| Capacity | HS200 Performance MLC MODE | | | |
|---|---|---|---|---|
| | Seq. Read (MB/s) | Seq. Write (MB/s) | Random Read 4KB (IOPS) | Random Write 4KB (IOPS) |
| 4 GB (native) No pre-configuration | 155 | 9.5 | 4890 | 980 |

| Capacity | DDR52 Performance MLC MODE | | | |
|---|---|---|---|---|
| | Seq. Read (MB/s) | Seq. Write (MB/s) | Random Read 4KB (IOPS) | Random Write 4KB (IOPS) |
| 4 GB (native) No pre-configuration | 95 | 9.5 | 4610 | 980 |

*(1) Test condition: Testmetrix VTESA-4100E; bus in x8 I/O mode.*

## 2.2 Power Consumption

**Table 2: Current Consumption**

| Test Item | Capacity | MLC | | | | | |
|---|---|---|---|---|---|---|---|
| | | ICCQ (mA) | | | ICC (mA) | | |
| | | DDR52 | HS200 | HS400 | DDR52 | HS200 | HS400 |
| **Write Current** | 4 GB (native) No pre-configuration | 29.10 | 31.00 | 31.10 | 22.50 | 22.50 | 22.70 |
| **Read Current** | | 33.90 | 39.30 | 48.40 | 22.30 | 37.40 | 37.30 |

*(1) Bus in x8 I/O mode; 25°C; $V_{CCQ}$ = 1.95 V in HS200 and HS400 $V_{CCQ}$ = 3.6V in DDR52. Measurements done as maximum RMS current consumption over 100 milliseconds.*

## 2.3 Data Reliability

- **Static and Dynamic Wear Leveling:** This feature eliminates overstressing Flash media by spreading the data writes across all Flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.
- **ECC**: Utilize LDPC ECC to provide correction of user data.
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

## 2.4 Failure Rate

**Table 3: Failure Rate**

| Failure Rate(1) | All capacities |
|---|---|
| FIT @55°C | 62.17 (153ball) |

*(1) The FIT data generated from high temperature experiment: Sample size = 77ea, 1 Lot.*

## 2.5 Environmental Conditions

**Table 4: Environmental Conditions and Test Conditions**

| Parameter | Value |
|---|---|
| Operating Temperature – Industrial Grade | -40°C to 85°C |
| Storage Temperature | -40°C to 85°C |

## 2.6 Endurance

**Table 5: Reliability Characteristics**

<table>
<tr><th colspan="2">Item</th><th colspan="2">Value</th></tr>
<tr><td colspan="2">Data Retention (@ 40˚C)</td><td colspan="2">10 years when 90% life remaining</td></tr>
<tr><td colspan="2"></td><td colspan="2">1 year when 10% life remaining</td></tr>
<tr><td rowspan="2">MLC mode Endurance[1]</td><td>100% Sequential Workload</td><td rowspan="2">4 GB (native)<br>No pre-configuration</td><td>10.5 TBW</td></tr>
<tr><td>JEDEC Enterprise Class Workload</td><td>1.65 TBW</td></tr>
<tr><td colspan="2">Data Reliability[2]</td><td colspan="2">< 1E-15 uncorrectable bit error rate</td></tr>
</table>

[1] Endurance is directly related to the User specific workload.

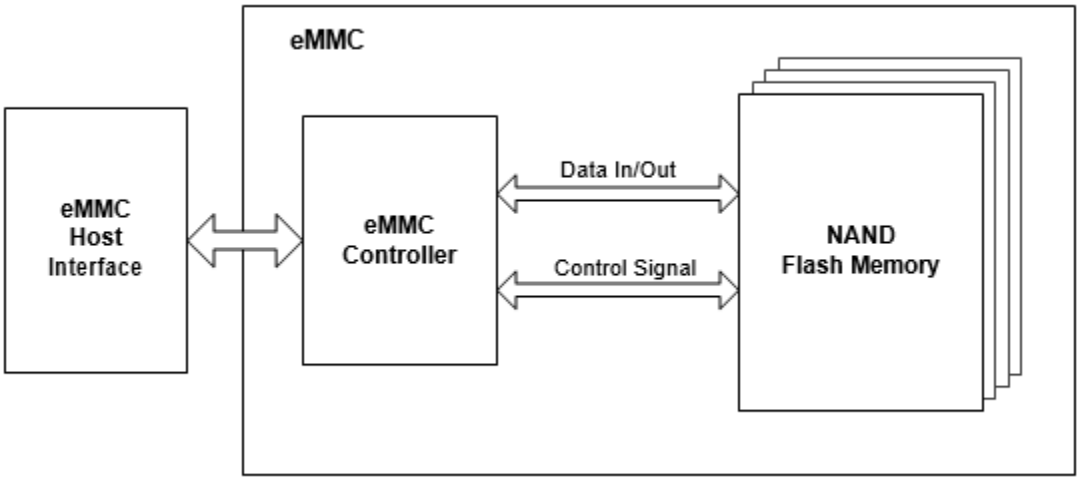
[2] Reference from JESD218

# 3 PRODUCT DESCRIPTION

The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

## 3.1 Functional Block Diagram

**Figure 1: eMMC Block Diagram**

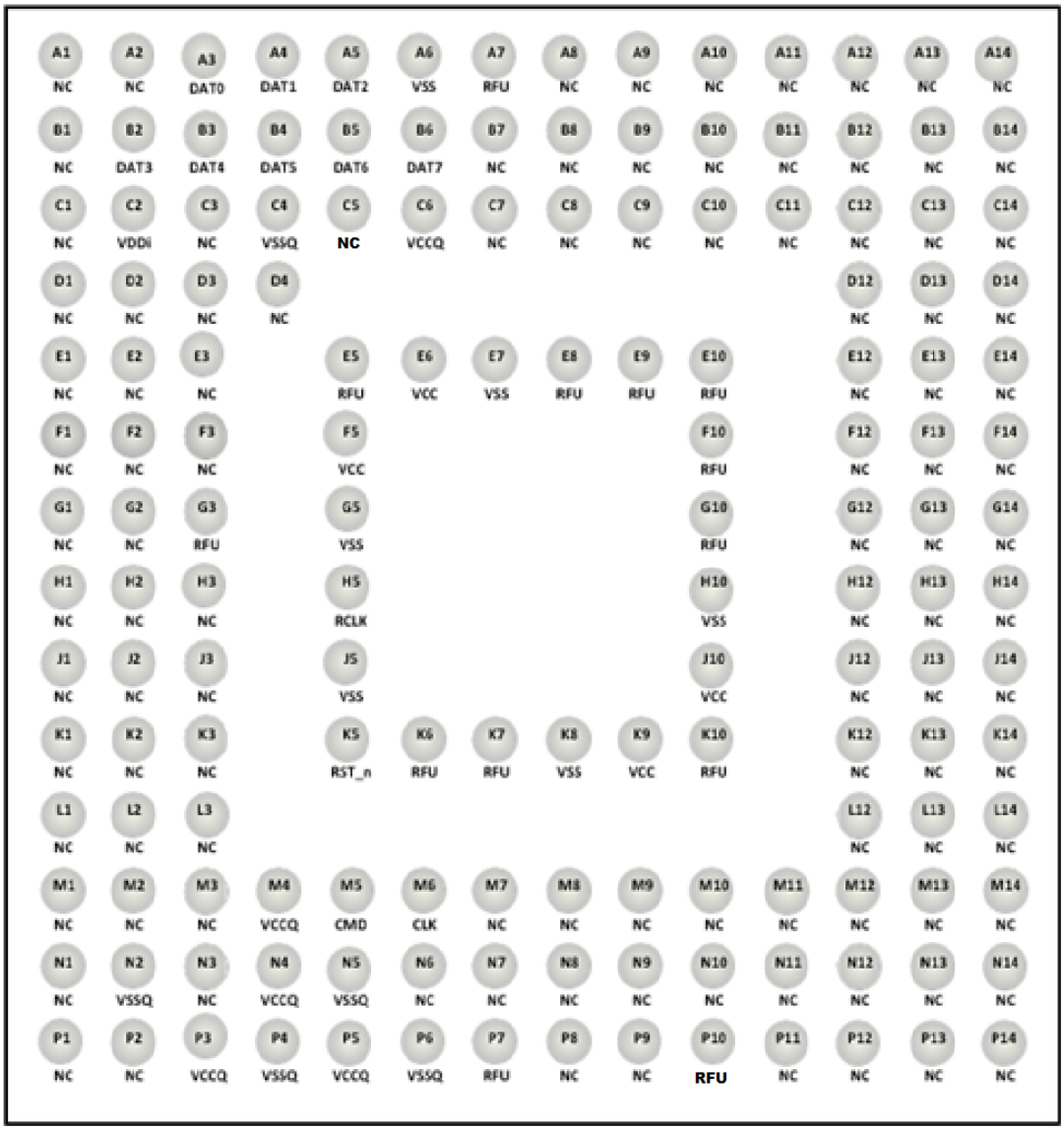


# 4 PACKAGE INFORMATION

## 4.1 Signal Interface

### 4.1.1 eMMC Ball-out Diagram

**Figure 2: 153-Ball Pin Assignments (Top View, Balls Down)***



### 4.1.2 Signal Descriptions

**Table 6: Signal Descriptions**

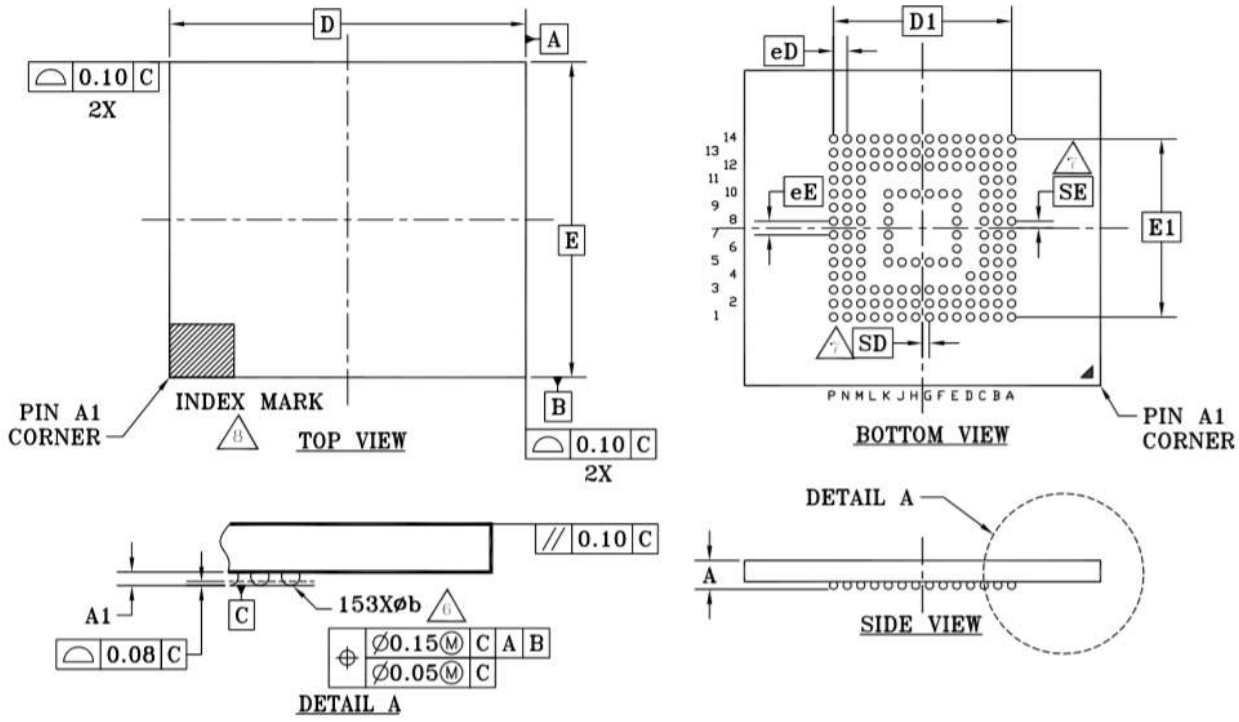
| Signal | Type | Description |
|---|---|---|
| CLK | Input | Clock.<br>Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency. |
| RCLK | Output | eMMC interface data strobe (HS400 mode) |
| CMD | I/O | Command.<br>This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host. |
| DA<br>T0<br>–<br>DA<br>T7 | I/O | Data I/O.<br>These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). eMMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Correspondingly, immediately after entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines. |
| RST_n | Input | Reset.<br>The RST_n signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. The host must set bits[1:0] in the extended CSD register [162] to 0x1 to enable this functionality before the host can use it. |
| VCC | Supply | NAND interface I/O and NAND Flash power supply. |
| VCCQ | Supply | eMMC controller core and eMMC interface I/O power supply. |
| VSS | Supply | NAND interface I/O and NAND Flash ground connection. |
| VSSQ | Supply | eMMC controller core and eMMC interface ground connection. |
| VDDi | - | Internal voltage node<br>0.1 µF x 1 and 2.2 µF x 1 capacitors are recommended for VDDi for core power stabilization.*<br>Do not tie to supply voltage or ground. |
| NC | - | No connect |
| RFU | - | Reserved for future use. Leave it floating. |

* A minimum of 1uF is required.

# 5 eMMC MECHANICAL SPECIFICATIONS

## 5.1 Package Dimensions

**Figure 3: 153-Ball BGA Dimensions – 11.5 mm x 13 mm x 0.8 mm**




| PACKAGE | TBD 153 | | | NOTE |
|---|---|---|---|---|
| JEDEC | MO-276 | | | |
| D X E | 13.00mm X 11.50mm PACKAGE | | | |
| SYMBOL | MIN. | NOM. | MAX. | |
| A | 0.70 | --- | 0.80 | PROFILE |
| A1 | 0.17 | --- | --- | BALL HEIGHT |
| D | 13.00 BSC | | | BODY SIZE |
| E | 11.50 BSC | | | BODY SIZE |
| D1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| E1 | 6.50 BSC | | | MATRIX FOOTPRINT |
| MD | 14 | | | MATRIX SIZE D DIRECTION |
| ME | 14 | | | MATRIX SIZE E DIRECTION |
| n | 153 | | | BALL COUNT |
| Ø b | 0.25 | 0.30 | 0.35 | BALL DIAMETER |
| eE | 0.50 BSC | | | BALL PITCH |
| eD | 0.50 BSC | | | BALL PITCH |
| SD / SE | 0.25 BSC | | | SOLDER BALL PLACEMENT |
| | D5-D11,E11-K11,L4-L11,E4-K4 F6-F9,G6-G9,H6-H9,J6-J9 | | | DEPOPULATED SOLDER BALLS |

NOTES:

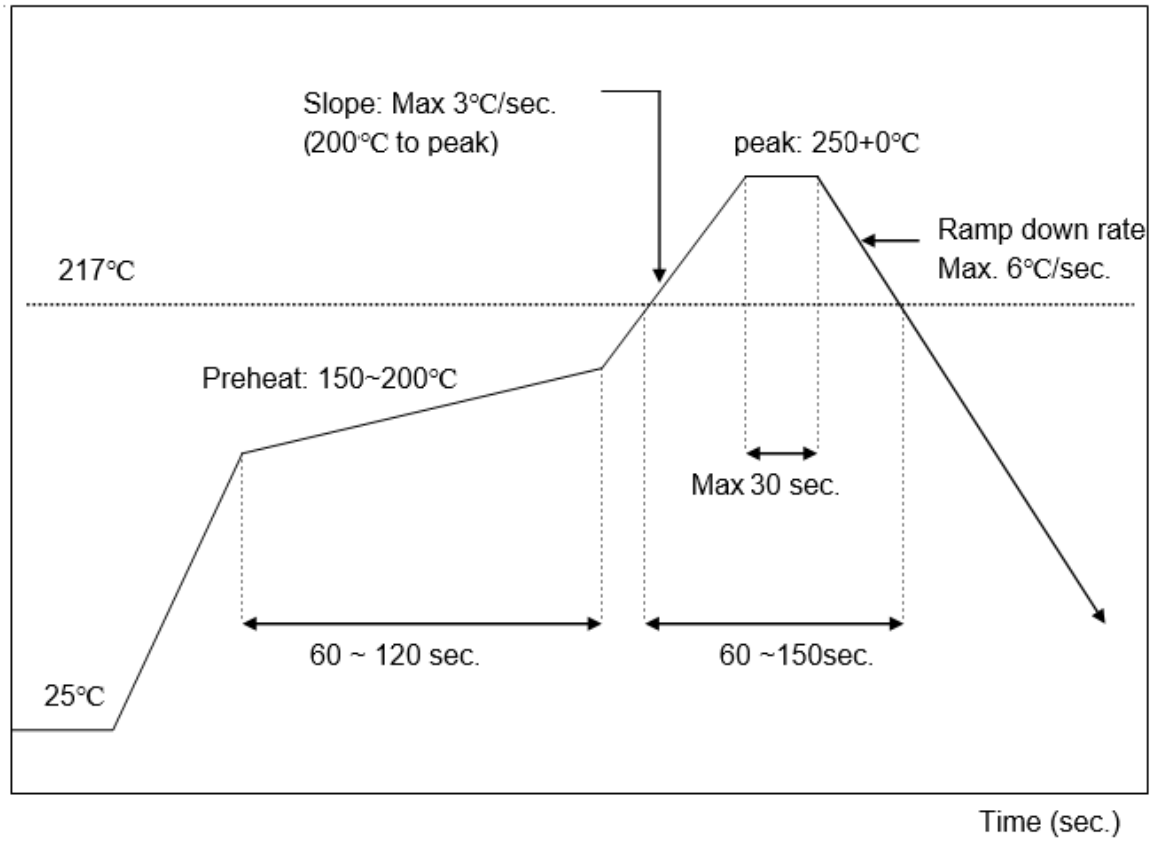
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP 95, SECTION 4.6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW D OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. TEST PADS MAY BE PRESENT BUT ARE NOT SHOWN. THEY ARE FOR INTERNAL USE ONLY AND ARE NOT SOLDER BALLS.

## 5.2 Recommended Reflow Profiles

**Table 7: Recommended Reflow Profile**

| Reflow Parameters | Suggested Range |
|---|---|
| Specifications: | IPC/JEDEC J-STD-020E |
| Average ramp-up rate (200℃ to peak): | 3 ℃/sec. max |
| Preheat: | 150~200℃, 60~120 seconds |
| Temperature maintained above 217℃: | 60~150 seconds |
| Time within 5℃ of actual peak temperature: | 30 seconds |
| Peak temperature: | 260+0℃ |
| Ramp-down rate: | 6℃/sec. max. |
| Time 25℃ to peak temperature: | 480 sec. max. |

**Figure 4: Recommended Reflow Profile**



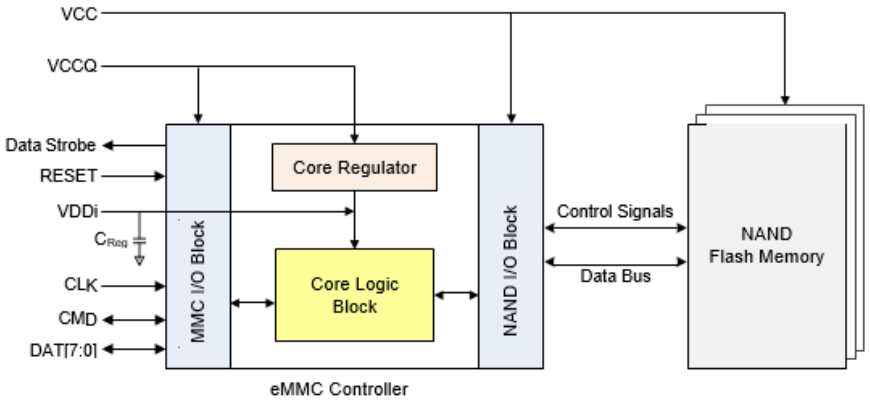
# 6 ELECTRICAL SPECIFICATION

## 6.1 Electrical Interface

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

$V_{CC}$ is used for the NAND Flash device and its interface voltage; $V_{CCQ}$ is used for the controller and the eMMC interface voltage.

**Figure 5: System Architecture**




## 6.2 DC Specifications

**Table 8: Power Requirements**

| Symbol | Parameter | Value (Minimum) | Value (Typical) | Value (Maximum) | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Voltage supply to Flash memory | 2.7 | 3.3 | 3.6 | V |
| $V_{CCQ}$ | Voltage supply to host interface | 2.7 (high range)<br>1.70 (low range) | 3.3 (high range)<br>1.80 (low range) | 3.6 (high range)<br>1.95 (low range) | V |
| $V_{DDi}$ | Internal voltage regulator connection to external capacitor | - | - | - | - |

**Figure 6: Recommended eMMC Connection**

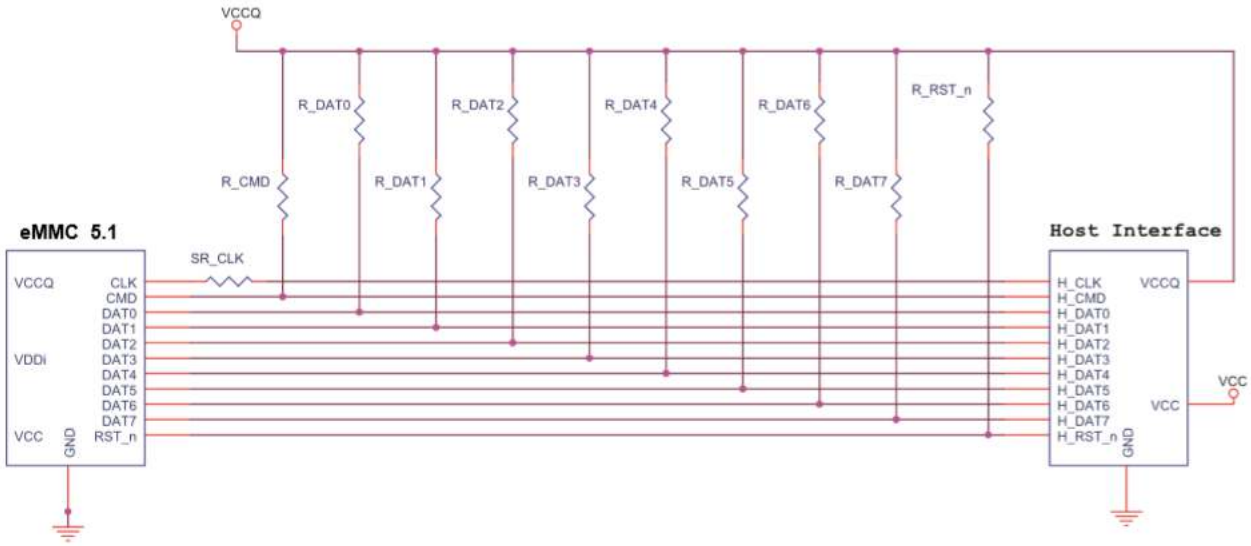



**Table 9: Recommended Capacitor and Resistor**

| Parameter | Symbol | Recommended | Comments |
|---|---|---|---|
| Pull-up resistance for CMD | R_CMD | 10 kΩ | To prevent bus floating. |
| Pull-up resistance for DAT[7:0] | R_DAT | 50 kΩ | To prevent bus floating. |
| Pull-up resistance for RST_n | R_RST_n | 50 kΩ | A pull-up resistance on the RST_n (H/W reset) line is not required if the host does not enable the H/W reset feature. |
| Series termination for CLK | SR_CLK | 22Ω | To stabilize the clock signal. It is recommend for customers to perform simulations using the controller IBIS model to confirm this value. |

Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.
- Recommended Value and Quantity:
  VCCQ: More than 0.1 µF x 1, 2.2 µF x 1 (for BGA153, this cap should be as close as possible to C6 ball), and 1 x 1 µF
  VCC: More than 0.1 µF x 1 and 2.2 µF x 1
  VDDi: More than 0.1 µF x 1 and 2.2 µF x 1
  A minimum of 1uF is required for VCCQ, VCC, and VDDi.

Customer is requested to place all of the caps shown above. For VCCQ caps, they should be located as close as possible to the VCCQ/VSSQ balls near the DAT0-7 signals.

# 7 REGISTER

The registers used in the SMART eMMC are shown in the table below. These registers are described in the sections that follow:

**Table 10: Supported Device Registers**

| Name | Width | Description |
|---|---|---|
| CID | 128 (Bits) | Card Identification |
| OCR | 32 (Bits) | Operation Condition Register |
| CSD | 128 (Bits) | Card Specific Data |
| ECSD | 512 (Bytes) | Extended Card Specific Data |

* The values in each register are based on MLC configuration.

## 7.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

**Table 11: CID Register Field Parameters**

| Name | Field | Width (Bits) | CID Bits | SMART CID Value |
|---|---|---|---|---|
| Manufacturer ID | MID | 8 | [127:120] | 0x01 |
| Reserved | - | 6 | [119:114] | -- |
| Device / BGA | CBX | 2 | [113:112] | 0x01 |
| OEM/application ID | OID | 8 | [111:104] | 0x00 |
| Product name | PNM | 48 | [103:56] | 0x533430303034 |
| Product revision | PRV | 8 | [55:48] | 0x01 |
| Product serial number | PSN | 32 | [47:16] | --(1) |
| Manufacturing date | MDT | 8 | [15:8] | --(2) |
| CRC7 checksum | CRC | 7 | [7:1] | --(3) |
| reserved | - | 1 | 0 | -- |

Note:

(2) Unique for each device. 32-bit unsigned binary integer.
(3) 2 hex digits for device manufacturing month and year.
(4) CRC for CID register. Different for each device.

## 7.2 OCR Register

The card identification (OCR) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

**Table 12: OCR Register Field Definitions**

| $V_{DD}$ Voltage Window | Width (Bits) | OCR Bits | OCR Value |
|---|---|---|---|
| Ready/Busy | 1 | [31] | card power up status bit (busy)(1) |
| Access Mode | 2 | [30:29] | 10b |
| Reserved | 5 | [28:24] | -- |
| 2.7-3.6V | 9 | [23:15] | 1 1111 1111b |
| 2.0-2.6V | 7 | [14:8] | 000 0000b |
| 1.70-1.95V | 1 | [7] | 1b |
| Reserved | 7 | [6:0] | -- |

Note:

(1) This bit is set to low if the device has not finished the power up routine.

## 7.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

**Table 13: CSD Register Field Parameters**

| Name | Field | Width (Bits) | CSD Bits | CSD Value |
|---|---|---|---|---|
| CSD structure | CSD_STRUCTURE | 2 | [127:126] | 0x03 |
| System specification version | SPEC_VERS | 4 | [125:122] | 0x04 |
| Reserved | -- | 2 | [121:120] | -- |
| Data read access time 1 | TAAC | 8 | [119:112] | 0x27 |
| Data read access time 2 in CLK cycles (NSAC x 100) | NSAC | 8 | [111:104] | 0x01 |
| Maximum bus clock frequency | TRAN_SPEED | 8 | [103:96] | 0x32 |
| Device command classes | CCC | 12 | [95:84] | 0xF5 |
| Maximum read data block length | READ_BL_LEN | 4 | [83:80] | 0x09 |
| Partial blocks for reads supported | READ_BL_PARTIAL | 1 | [79] | 0x00 |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | [78] | 0x00 |
| Read block misalignment | READ_BLK_MISALIGN | 1 | [77] | 0x00 |
| DSR implemented | DSR_IMP | 1 | [76] | 0x00 |
| Reserved | -- | 2 | [75:74] | -- |
| Device size | C-SIZE | 12 | [73:62] | 0xFFF |
| Maximum read current as VDD,min | VDD_R_CURR_MIN | 3 | [61:59] | 0x07 |
| Maximum read current as VDD,max | VDD_R_CURR_MAX | 3 | [58:56] | 0x07 |
| Maximum write current as VDD,min | VDD_W_CURR_MIN | 3 | [55:53] | 0x07 |
| Maximum write current as VDD,max | VDD_W_CURR_MAX | 3 | [52:50] | 0x07 |
| Device size multiplier | C-SIZE_MULT | 3 | [49:47] | 0x07 |
| Erase group size | ERASE_GRP_SIZE | 5 | [46:42] | 0x1F |
| Erase group size multiplier | ERASE_GRP_SIZE_MULT | 5 | [41:37] | 0x1F |
| Write protect group size | WP_GRP_SIZE | 5 | [36:32] | 0x0F |
| Write protect group enable | WP_GRP_ENABLE | 1 | [31] | 0x01 |
| Manufacturer default ECC | DEFAULT_ECC | 2 | [30:29] | 0x00 |
| Write-speed factor | R2W_FACTOR | 3 | [28:26] | 0x02 |
| Maximum write data block length | WRITE_BL_LEN | 4 | [25:22] | 0x09 |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | [21] | 0x00 |
| Reserved | -- | 4 | [20:17] | -- |
| Content protection application | CONTENT_PROT_APP | 1 | [16] | 0x00 |
| File-format group | FILE_FORMAT_GRP | 1 | [15] | 0x00 |
| Copy flag (OTP) | COPY | 1 | [14] | 0x00 |

| Name | Field | Width (Bits) | CSD Bits | CSD Value |
|---|---|---|---|---|
| Permanent write protection | PERM_WRITE_PROTECT | 1 | [13] | 0x00 |
| Temporary write protection | TEMP_WRITE_PROTECT | 1 | [12] | 0x00 |
| File format | FILE_FORMAT | 2 | [11:10] | 0x00 |
| ECC code | ECC | 2 | [9:8] | 0x00 |
| CRC | CRC | 7 | [7:1] | -- |
| Not used; always 1 | -- | 1 | [0] | -- |

## 7.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

**Table 14: ECSD Register Field Parameters**

| Name | Field | Size (Bytes) | Cell Type[1] | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| Reserved | -- | 6 | -- | [511:506] | -- |
| Extended Security Commands Error | EXT_SECURITY_ERR | 1 | R | [505] | 0x00 |
| Supported command sets | S_CMD_SET | 1 | R | [504] | 0x01 |
| HPI features | HPI_FEATURES | 1 | R | [503] | 0x01 |
| Background operations support | BKOPS_SUPPORT | 1 | R | [502] | 0x01 |
| Max packed read commands | MAX_PACKED_READS | 1 | R | [501] | 0x3F |
| Max packed write commands | MAX_PACKED_WRITES | 1 | R | [500] | 0x3F |
| Data tag support | DATA_TAG_SUPPORT | 1 | R | [499] | 0x01 |
| Tag unit size | TAG_UNIT_SIZE | 1 | R | [498] | 0x00 |
| Tag resources size | TAG_RES_SIZE | 1 | R | [497] | 0x00 |
| Context management capabilities | CONTEXT_CAPABILITIES | 1 | R | [496] | 0x78 |
| Large unit size | LARGE_UNIT_SIZE_M1 | 1 | R | [495] | 0x01 |
| Extended partitions attribute support | EXT_SUPPORT | 1 | R | [494] | 0x03 |
| Supported Modes | SUPPORTED_MODES | 1 | R | [493] | 0x01 |
| FFU features | FFU_FEATURES | 1 | R | [492] | 0x00 |
| Operations code timeout | OPERATION_CODE_TIMEOUT | 1 | R | [491] | 0x17 |
| FFU Argument | FFU_ARG | 4 | R | [490:487] | 0xFFFAFFF0 |
| Reserved | -- | 181 | -- | [486:306] | -- |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4 | R | [305:302] | 0x00 |
| Vendor proprietary health report | VENDOR_PROPRIETARY_HEALTH_REPORT | 32 | R | [301:270] | 0x00 |
| Device life time estimation type B | DEVICE_LIFE_TIME_EST_TYP_B | 1 | R | [269] | Variable |
| Device life time estimation type A | DEVICE_LIFE_TIME_EST_TYP_A | 1 | R | [268] | Variable |
| Pre EOL information | PRE_EOL_INFO | 1 | R | [267] | Variable |
| Optimal read size | OPTIMAL_READ_SIZE | 1 | R | [266] | 0x40 |
| Optimal write size | OPTIMAL_WRITE_SIZE | 1 | R | [265] | 0x40 |
| Optimal trim unit size | OPTIMAL_TRIM_UNIT_SIZE | 1 | R | [264] | 0x07 |
| Device Version | Device version | 2 | R | [263:262] | 0x3405 |

| Name | Field | Size (Bytes) | Cell Type[1] | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| Firmware version | FIRMWARE_VERSION | 8 | R | [261:254] | --[1] |
| Power class for200MHz, DDR at VCC=3.6V | PWR_CL_DDR_200_360 | 1 | R | [253] | 0x00 |
| Cache size | CACHE_SIZE | 4 | R | [252:249] | 0x400 |
| Generic CMD6 timeout | GENERIC_CMD6_TIME | 1 | R | [248] | 0x05 |
| Power off notification (long) timeout | POWER_OFF_LONG_TIME | 1 | R | [247] | 0x64 |
| Background operations status | BKOPS_STATUS | 1 | R | [246] | 0x00 |
| Number of correctly programmed sectors | CORRECTLY_PRG_SECTORS_NUM | 4 | R | [245:242] | 0x00 |
| First initialization time after partitioning | INI_TIMEOUT_AP | 1 | R | [241] | 0x0A |
| Reserved | -- | 1 | -- | [240] | -- |
| Power class for 52 MHz, DDR at 3.6V | PWR_CL_DDR_52_360 | 1 | R | [239] | 0x00 |
| Power class for 52 MHz, DDR at 1.95V | PWR_CL_DDR_52_195 | 1 | R | [238] | 0x00 |
| Power class for 200 MHz at 1.95V, VCC = 3.6V | PWR_CL_200_195 | 1 | R | [237] | 0x00 |
| Power class for 200 MHz at 1.3V, VCC = 3.6V | PWR_CL_200_130 | 1 | R | [236] | 0x00 |
| Minimum write performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_W_8_52 | 1 | R | [235] | 0x00 |
| Minimum read performance for 8-bit at 52 MHz in DDR mode | MIN_PERF_DDR_R_8_52 | 1 | R | [234] | 0x00 |
| Reserved | -- | 1 | -- | [233] | -- |
| TRIM multiplier | TRIM_MULT | 1 | R | [232] | 0x02 |
| Secure feature support | SEC_FEATURE_SUPPORT | 1 | R | [231] | 0x55 |
| SECURE ERASE multiplier | SEC_ERASE_MULT | 1 | R | [230] | 0xFF |
| SECURE TRIM multiplier | SEC_TRIM_MULT | 1 | R | [229] | 0xFF |
| Boot information | BOOT_INFO | 1 | R | [228] | 0x07 |
| Reserved | -- | 1 | -- | [227] | -- |
| Boot partition size | BOOT_SIZE_MULT | 1 | R | [226] | 0x20 |
| Access size | ACC_SIZE | 1 | R | [225] | 0x06 |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 0x01 |
| High-capacity erase timeout | ERASE_TIMEOUT_ | 1 | R | [223] | 0x02 |

| Name | Field | Size (Bytes) | Cell Type(1) | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| | MULT | | | | |
| Reliable write-sector count | REL_WR_SEC_C | 1 | R | [222] | 0x01 |
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | R | [221] | 0x10 |
| Sleep current ($V_{CC}$) | S_C_VCC | 1 | R | [220] | 0x07 |
| Sleep current ($V_{CCQ}$) | S_C_VCCQ | 1 | R | [219] | 0x07 |
| Production state awareness timeout | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1 | R | [218] | 0x17 |
| Sleep/awake timeout | S_A_TIMEOUT | 1 | R | [217] | 0x13 |
| Sleep Notification Timeout | SLEEP_NOTIFICATION_TIME | 1 | R | [216] | 0x0C |
| Sector count | SEC-COUNT | 4 | R | [215:212] | 0x00748000 |
| Reserved | -- | 1 | -- | [211] | -- |
| Minimum write performance for 8-bit at 52 MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 0x00 |
| Minimum read performance for 8-bit at 52 MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 0x00 |
| Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 0x00 |
| Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 0x00 |
| Minimum write performance for 4-bit at 26 MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 0x00 |
| Minimum read performance for 4-bit at 26 MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 0x00 |
| Reserved | -- | 1 | -- | [204] | -- |
| Power class for 26 MHz at 3.6V 1 R | PWR_CL_26_360 | 1 | R | [203] | 0x00 |
| Power class for 52 MHz at 3.6V 1 R | PWR_CL_52_360 | 1 | R | [202] | 0x00 |
| Power class for 26 MHz at 1.95V 1 R | PWR_CL_26_195 | 1 | R | [201] | 0x00 |
| Power class for 52 MHz at 1.95V 1 R | PWR_CL_52_195 | 1 | R | [200] | 0x00 |
| Partition switching timing | PARTITION_SWITCH_TIME | 1 | R | [199] | 0x06 |
| Out-of-interrupt busy timing | OUT_OF_INTERRUPT_TIME | 1 | R | [198] | 0x05 |
| I/O driver strength | DRIVER_STRENGTH | 1 | R | [197] | 0x1F |

| Name | Field | Size (Bytes) | Cell Type[1] | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| Card type | CARD_TYPE | 1 | R | [196] | 0x57 |
| Reserved | -- | 1 | -- | [195] | -- |
| CSD structure version | CSD_STRUCTURE | 1 | R | [194] | 0x02 |
| Reserved | -- | 1 | -- | [193] | -- |
| Extended CSD revision | EXT_CSD_REV | 1 | -- | [192] | 0x08 |
| Command set | CMD_SET | 1 | R/W/E_P | [191] | 0x00 |
| Reserved | -- | 1 | -- | [190] | -- |
| Command set revision | CMD_SET_REV | 1 | R | [189] | 0x00 |
| Reserved | -- | 1 | -- | [188] | -- |
| Power class | POWER_CLASS | 1 | R/W/E_P | [187] | 0x00 |
| Reserved | -- | 1 | -- | [186] | -- |
| High-speed interface timing | HS_TIMING | 1 | R/W/E_P | [185] | 0x00 |
| Reserved | -- | 1 | -- | [184] | -- |
| Bus width mode | BUS_WIDTH | 1 | W/E_P | [183] | 0x00 |
| Reserved | -- | 1 | -- | [182] | -- |
| Erased memory content | ERASED_MEM_CONT | 1 | R | [181] | 0x00 |
| Reserved | -- | 1 | -- | [180] | -- |
| Partition configuration | PARTITION_CONFIG | 1 | R/W/E, R/W/E_P | [179] | 0x00 |
| Boot config protection | BOOT_CONFIG_PROT | 1 | R/W, R/W/C_P | [178] | 0x00 |
| Boot bus Conditions | BOOT_BUS_CONDITIONS | 1 | R/W/E | [177] | 0x00 |
| Reserved | -- | 1 | -- | [176] | -- |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W/E_P | [175] | 0x00 |
| Boot write protection status registers | BOOT_WP_STATUS | 1 | R | [174] | 0x00 |
| Boot area write protection register | BOOT_WP | 1 | R/W, R/W/C_P | [173] | 0x00 |
| Reserved | -- | 1 | - | [172] | -- |
| User write protection register | USER_WP | 1 | R/W, R/W/C_P, R/W/E_P | [171] | 0x00 |
| Reserved | -- | 1 | -- | [170] | -- |

| Name | Field | Size (Bytes) | Cell Type[1] | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| Firmware configuration | FW_CONFIG | 1 | R/W | [169] | 0x00 |
| RPMB size | RPMB_SIZE_MULT | 1 | R | [168] | 0x20 |
| Write reliability setting register | WR_REL_SET | 1 | R/W | [167] | 0x1F |
| Write reliability parameter register | WR_REL_PARAM | 1 | R | [166] | 0x15 |
| Start sanitize operation | SANITIZE_START | 1 | W/E_P | [165] | 0x00 |
| Manually start background operations | BKOPS_START | 1 | W/E_P | [164] | 0x00 |
| Enable background operations handshake | BKOPS_EN | 1 | R/W | [163] | 0x00 |
| Hardware reset function | RST_n_FUNCTION | 1 | R/W | [162] | 0x00 |
| HPI management | HPI_MGMT | 1 | R/W/E/P | [161] | 0x00 |
| Partitioning support | PARTITIONING_SUPPORT | 1 | R/W/E, R/W/E_P | [160] | 0x07 |
| Maximum enhanced area size | MAX_ENH_SIZE_MULT | 3 | R | [159:157] | 0x0000E9 |
| Partitions attribute | PARTITIONS_ATTRIBUTE | 1 | R/W | [156] | 0x00 |
| Partitioning setting | PARTITIONING_SETTING-COMPLETED | 1 | R/W | [155] | 0x00 |
| General-purpose partition size | GP_SIZE_MULT | 12 | R/W | [154:143] | 0x00 |
| Enhanced user data area size | ENH_SIZE_MULT | 3 | R/W | [142:140] | 0x00 |
| Enhanced user data start address | ENH_START_ADDR | 4 | R/W | [139:136] | 0x00 |
| Reserved | - | 1 | - | [135] | -- |
| Bad block management mode | SEC_BAD_BLK_MGMNT | 1 | R/W | [134] | 0x00 |
| Production state awareness | PRODUCTION_STATE_AWARENESS | 1 | R/W/E | [133] | 0x00 |
| Package case temperature is controlled | TCASE_SUPPORT | 1 | W/E_P | [132] | 0x00 |
| Periodic wake-up | PERIODIC_WAKEUP | 1 | R/W/E | [131] | 0x00 |
| Program CID/CSD in DDR mode support | PROGRAM_CID_CSD_DDR_SUPPORT | 1 | R | [130] | 0x00 |
| Reserved | - | 2 | - | [129:128] | -- |
| Vendor specific fields | VENDOR_SPECIFIC_NFIELD | 64 | <vs> | [127:64] | 0x00 |
| Native sector size | NATIVE_SECTOR_SIZE | 1 | R | [63] | 0x01 |
| Sector size emulation | USE_NATIVE_SECTOR | 1 | R/W | [62] | 0x00 |

| Name | Field | Size (Bytes) | Cell Type(1) | ECSD Bytes | ECSD Values |
|---|---|---|---|---|---|
| Sector size | DATA_SECTOR_SIZE | 1 | R | [61] | 0x00 |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU | 1 | R | [60] | 0x0A |
| Class 6 command control | CLASS_6_CTRL | 1 | R/W/E_P | [59] | 0x00 |
| Number of addressed groups to be released | DYNCAP_NEEDED | 1 | R | [58] | 0x00 |
| Exception events control | EXCEPTION_EVENTS_CTRL | 2 | R/W/E_P | [57:56] | 0x00 |
| Exception events status | EXCEPTION_EVENTS_STATUS | 2 | R | [55:54] | 0x00 |
| Extended partitions attribute | EXT_PARTITIONS_ATTRIBUTE | 2 | R/W | [53:52] | 0x00 |
| Context configuration | CONTEXT_CONF | 15 | R/W/E_P | [51:37] | 0x00 |
| Packed command status | PACKED_COMMAND_STATUS | 1 | R | [36] | 0x00 |
| Packed command failure index | PACKED_FAILURE_INDEX | 1 | R | [35] | 0x00 |
| Power off notification | POWER_OFF_NOTIFICATION | 1 | R/W/E_P | [34] | 0x00 |
| Control to turn the cache on/off | CACHE_CTRL | 1 | R/W/E_P | [33] | 0x00 |
| Flushing of the cache | FLUSH_CACHE | 1 | W/E_P | [32] | 0x00 |
| Control to turn the Barrier ON/OFF | BARRIER_CTRL | 1 | R/W | [31] | 0x00 |
| Mode config | MODE_CONFIG | 1 | R/W/E_P | [30] | 0x00 |
| Mode operation codes | MODE_OPERATION_CODES | 1 | W/E_P | [29] | 0x00 |
| Reserved | - | 2 | - | [28:27] | -- |
| FFU status | FFU_STATUS | 1 | R | [26] | 0x00 |
| Pre loading data size | PRE_LOADING_DATA_SIZE | 4 | R/W/E_P | [25:22] | 0x00 |
| Max pre loading data size | MAX_PRE_LOADING_DATASIZE | 4 | R | [21:18] | 0x00748000 |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ ENABLEMENT | 1 | R/W/E & R | [17] | 0x01 |
| Secure removal type | SECURE_REMOVAL_TYPE | 1 | R/W & R | [16] | 0x3B |
| Reserved | - | 16 | - | [15:0] | -- |

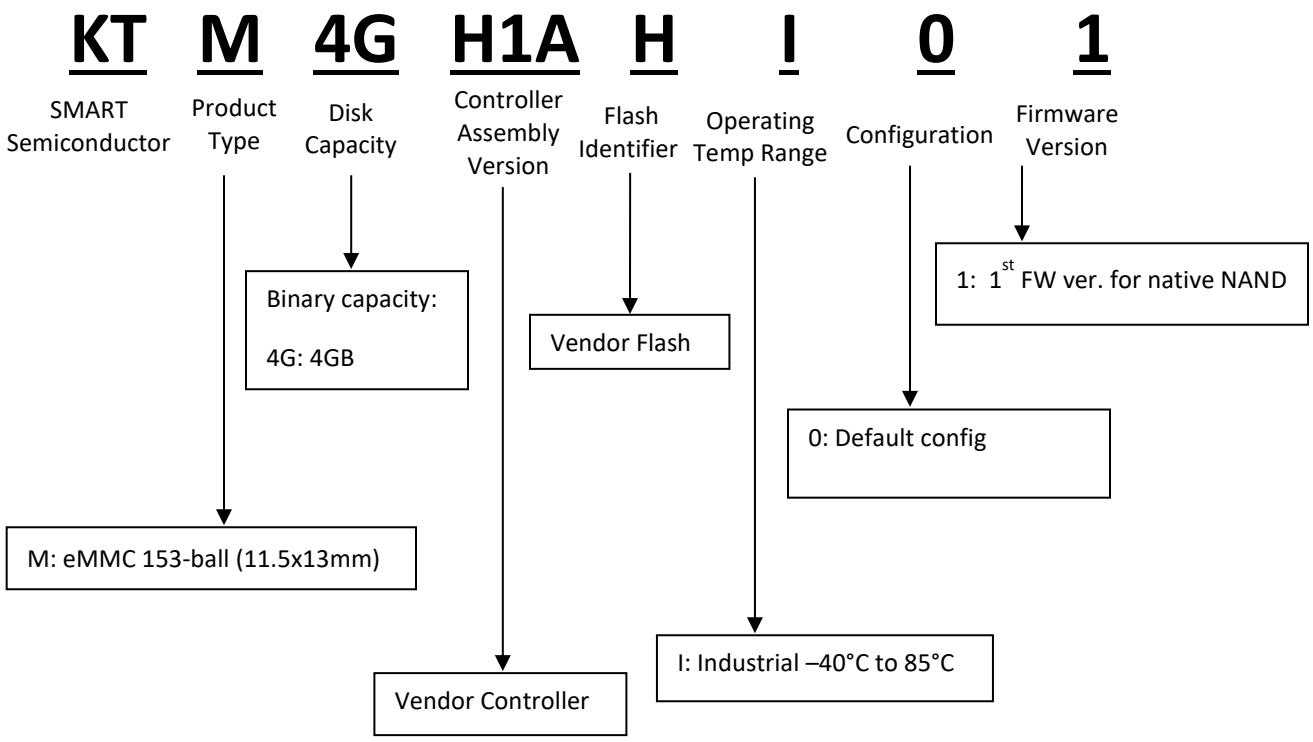
(1) Note: FIRMWARE_VERSION depends on capacity.

# 8 PART NUMBERS

**Table 14: Part Numbering Information**

| Capacity | Part Number |
|---|---|
| 4GB | KTM4GH1AHI01 |

## 8.1 Part Number Decoder




***Note:***

[1] Actual Firmware Revision as reported in ECSD [257:254] in ASCII

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