SMARTsemi Qualification and Reliability Report

Automotive Grade eMMC 153b

March 2023
Rev 0.1

REVISION HISTORY

Date	Revision	Section(s)	Description
March 2023	0.1	All	Initial Release

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1 PRODUCT INFORMATION

Product Name	eMMC
Grade Temp.	AEC-Q100 Grade 2 (-40 ~ 105°C)
Package	153-balls (11.5*13.0*1.0mm)
Part Number	KTM8GP1CWW01 KTMAGP1CWW01 KTMBGP1CWW01

2 RESULT OVERVIEW

TEST GROUP A-ACCELERATED ENVIRONMENT STRESS TESTS					
Test Item		Test Reference	Sample Size/Lot	Number of Lots	Test Result
3-1	Pre-condition Test (PC)	JEDEC/ JESD22 A113 AEC-Q100 -#A1	693	-	Pass
3-2	High Acceleration Stress Test (HAST with bias)	JEDEC/ JESD22 A110 AEC-Q100 -#A2	77	3	Pass
3-3	High Acceleration Stress Test (HAST unbias)	JEDEC/ JESD22 A118 AEC-Q100 -#A3	77	3	Pass
3-3	Temperature Cycling Test (TCT)	JEDEC/ JESD22 A104 AEC-Q100 - #A4	77	3	Pass
3-4	High Temperature Storage Life Test(HTSL)	JEDEC/ JESD22 A103 AEC-Q100 -#A6	45	2	Pass
			25	1	
TEST GROUP B-ACCELERATED LIFETIME SIMULATION TESTS					
Test Item		Test Reference	Sample Size/Lot	Number of Lots	Test Result
4-1	Early Life Failure Rate(ELFR)	AEC-Q100-008 AEC-Q100 -#B2	800	3	Pass
4-2	Low Temperature Data Retention(LTDR)	AEC-Q100-005 AEC-Q100 -#B3	77	3	Pass
4-3	High Temperature Operating Life(HTOL)	JEDEC/ JESD22 A108 AEC-Q100 -#B1	77	2	Pass
4-4	High Temperature Data Retention(HTDR)	AEC-Q100-005 AEC-Q100 -#B3	77	2	Pass

TEST GROUP C-PACKAGE ASSEMBLY INTEGRITY TESTS					
Test Item		**Test Reference**	**Sample Size/Lot**	**Number of Lots**	**Test Result**
5-1	Wire Bond Shear (WBS)	AEC Q100-001 AEC_Q003 AEC-Q100 -#C1	30 bonds from a minimum 5 devices		Pass
5-2	Wire Bond Pull (WBP)	MIL-STD-883, Method 2011, AEC_Q003 AEC-Q100 -#C2			Pass
5-3	Solderability Test	JEDEC/ J-STD-002D AEC-Q100 -#C3	15	1	Pass
5-4	Physical Dimensions	JEDEC/ JESD22-B100 AEC_Q003 AEC-Q100 -#C4	10	3	Pass
5-5	Solder Ball Shear	AEC-Q100-010 AEC-Q100 -#C5	5 balls from a minimum 10 devices	3	Pass
TEST GROUP E-ELECTRICAL VERIFICATION TESTS					
Test Item		**Test Reference**	**Sample Size/Lot**	**Number of Lots**	**Test Result**
6-1	ESD Test (Human-Body Model, HBM)	AEC-Q100-002 AEC-Q100 -#E2	3	1	Pass
6-2	ESD Test (Charged Device Model, CDM)	AEC-Q100-011 AEC-Q100 -#E3	3	1	Pass
6-3	Latch Up	AEC-Q100-004 AEC-Q100 -#E4	6	1	Pass

3 ACCELERATED ENVIRONMENT STRESS TESTS

3.1 Pre-condition Test (PC)

Purpose:

This Test Method establishes an industry standard preconditioning flow for non-thematic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in- house reliability testing (qualification and reliability monitoring) to evaluate long term reliability(which might be impacted by solder reflow).

Test Condition(s):

- Step1: External Visual & Function Test and SAT Inspection
- Step2: Temperature Cycle Test (-65 ℃/150 ℃, 5 cycles)
- Step3: High temperature Storage Baking (125 ℃, 24 hours)
- Step4: Moisture soak (60℃/60% RH, 40 hours)
- Step5: IR Reflow * 3 times(260℃)
- Step6: External Visual & Function Test and SAT Inspection
- Test Reference: JESD22-A113

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 693	NA

Criteria : Acc/Rej = 0/1

3.2 High Acceleration Stress Test (HAST with bias)

Purpose:

The HAST test is employed to evaluate the endurance of semiconductor devices used and stored in high temperature and high humidity ambience, and to provide for a method of accelerated evaluation of the reliability of non-hermetic packaged devices due to humidity, as well as evaluation of the influence of humidity applied on the devices when submitted to accelerated conditions.

Test Condition(s):

- Pre-condition
- 110°C, 85%RH, Vcc,max, 264hours
- Each device test and all pass by VI and FT
- Sample size: 3 Lots, 231ea
- Test Reference: JEDS22-A110

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

3.3 High Acceleration Stress Test (HAST/unbias)

Purpose:

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermeticpackaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or alongthe interface between the external protective material and the metallic conductors which passthrough it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is is used to identifyfailure mechanisms internal to the package and is destructive.

Test Condition(s):

- Pre-condition
- 110°C, 85%RH, 264hours
- Each device test and all pass by VI and FT
- Sample size: 3 Lots, 231ea
- Test Reference: JEDS22-A118

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

3.4 Temperature Cycling Test (TCT)

Purpose:

This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst caseload temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

Test Condition(s):

- Pre-condition
- -65°C~150°C, Transition time: 10minutes, Dwell time=5minutes
- Test Duration: 500 cycles
- Each device test and all pass by VI and FT
- Sample size: 3 Lots, 231ea
- AEC-Q100 Grade 1
- Test Reference: JEDS22-A104

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

3.5 High Temperature Storage Life Test (HTSL)

Purpose:

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time tofailure distributions of solid state electronic devices, including non-volatile memory devices (data retention failure mechanisms). Thermally activated failure mechanisms are modeled usingthe Arrhenius Equation for acceleration. During the test, accelerated stress temperatures are used without electrical conditions applied. This test may be destructive, depending on time, temperature and packaging (if any).

Test Condition(s):

- High ambient temperature = 150°C
- Test Duration: 1000hours
- Sample size: 3 Lots, 115ea (45ea/Lot, 25ea/Lot)
- AEC-Q100 Grade 1
- Test Reference: JESD22-A103

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 115	NA

Criteria: Acc/Rej = 0/1

4 ACCELERATED LIFETIME SIMULATION TESTS

4.1 Early Life Failure Rate (ELFR)

Purpose:

The ELFR test is to evaluate the endurance of devices when they are submitted to electrical stressand thermal stress over an extended time period.

Test Condition(s):

- Pre-condiction Program/Erase Endurance with 300/ 3K cycles
- High ambient temperature = 125°C
- Test Duration: 48 hours
- Vstress=3.63V
- Sample size: 3 Lots, 2400ea (800ea/Lot)
- AEC-Q100 Grade 1
- Test Reference: AEC-Q100-008

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 2400	NA

Criteria: Acc/Rej = 0/1

4.2 Low Temperature Data Retention (LTDR)

Purpose:

The low-temperature data retention is performed for the purpose of the reliability of dataretention in a lifetime.

Test Condition(s):

- Pre-condiction Program/Erase Endurance with 300/ 3K cycles
- High ambient temperature = 55°C
- Test Duration: 1000hours with 300/ 3K cycles
- Sample size: 3 Lots, 231ea (77ea/Lot)
- AEC-Q100 Grade 3
- Test Reference: AEC-Q100-005

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

4.3 High Temperature Operating Life(HTOL)

Purpose:

The HTOL test is to evaluate the endurance of devices when they are submitted to electricalstress and thermal stress over an extended time period.

Test Condition(s):

- Pre-condiction Program/Erase Endurance with 300/ 3K cycles
- High ambient temperature = 125°C
- Test Duration: 1000hours
- Vstress=3.63V
- Sample size: 2 Lots, 154ea (77ea/Lot)
- AEC-Q100 Grade 1
- Test Reference: JESD22-A108

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

4.4 High Temperature Data Retention (HTDR)

Purpose:

The high-temperature data retention is performed for the purpose of the reliability of dataretention in a life time.

Test Condition(s):

- Pre-condiction Program/Erase Endurance with 300/ 3K cycles
- High ambient temperature = 125°C
- Test Duration: 10 hours with 3K cycles, 100 hours with 300 cycles
- 300 cycles 125C 100hrs, equivalent 40°C for 10 years& 3K cycles 125C 10hrs, equivalent 40°C for 1 year
- Sample size: 2 Lots, 154ea (77ea/Lot)
- AEC-Q100 Grade 2
- Test Reference: AEC-Q100-005

Test Result:

Product	Result	Remark
eMMC 153-balls	0 Fail / 231	NA

Criteria: Acc/Rej = 0/1

5 PACKAGE ASSEMBLY INTEGRITY TESTS

5.1 Wire Bond Shear (WBS)

Purpose:

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a package bonding surface, or an aluminum wedge/stitch bond and a package bonding surface, on either pre-encapsulation or post-encapsulation devices.

This strength measurement is extremely important in determining two features:

1) The integrity of the metallurgical bond which has been formed.
2) The reliability of gold and aluminum wire bonds to die or package bonding surfaces.

Test Condition(s):

- 30 bonds from minimum 5 units
- Sample size: 5ea/Lot , 30 bonds/ea, Total: 150bonds
- Test speed: 100um/sec
- Shear height: 3 um
- Test minimum bond stress (grams force): bigger than 12.6 grams for wire bond is 0.8mil.
- Test Reference: AEC Q100-001, AEC_Q003

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	Cpk>1.67	PASS

5.2 Wire Bond Pull (WBP)

Purpose:

The test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document.This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds externalto the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam leador flip chip devices.

Test Condition(s):

- After TCT, 30 bonds from minimum 5 units
- Sample size: 5ea/ Lot , 30 bonds/ea, Total: 150bonds
- Test speed: 600um/sec
- Test minimum bond stress (grams force): bigger than 1.7 grams for wire bond is 0.8mil.
- Test Reference: MIL-STD-883, Method 2011, AEC_Q003

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	Cpk>1.67	PASS

5.3 Solderability Test (SD)

Purpose:

The purpose of this test method is to evaluate the solderability of terminations that are normally joined by a soldering operation

Test Condition(s):

- 8 hours steam aging (water vapor 93 °C +3 °C /-5 °C)
- Temperature=245±5℃
- Dwell time=5±0.5 sec
- Sample size: 15ea/Lot, Total: 15ea
- Test Reference: J-STD-002D

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	>95% lead coverage	PASS

5.4 Physical Dimensions (PD)

Purpose:

The test is to measure samples' coplanarity.

Test Condition(s):

- Sample size: 3 Lots, 10ea/Lot, Total: 30ea
- Test reference: JESD22-B100, AEC_Q003

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	Cpk>1.67	PASS

5.5 Solder Ball Shear (SBS)

Purpose:

The purpose of this test method is to define the procedure for measuring the shear strength of the interface between the barrier metal and solder ball. This method also establishes the minimum shear strength requirements for this interface.

Test Condition(s):

- Two reflow 220 °C before Solder Ball Shear
- Solder ball shear strength shall be 3200 gram/mm2 in conjunction with acceptable separation modes.
- Sample size: 3 Lots, 10ea/Lot, 5 balls/ea, Total: 150balls
- Test speed: 280um/sec
- Shear height: 50um
- Ball height: 0.15mm
- Test minimum ball stress (grams force): greater than 197 grams for barrier metal diameteris 0.275mm
- Test Reference: : AEC-Q100-010, AEC_Q003

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	Cpk>1.67	PASS

6 ELECTRICAL VERIFICATION TESTS

6.1 ESD TEST (Human Body Model, HBM)

Purpose:

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposureto a defined human body model (HBM) electrostatic discharge (ESD). The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatabledata will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

Test Condition(s):

- Resistor: 1.5kΩ, Capacitor: 100 pF
- 500V~ 2000V(±), Step: 250V(±)
- Sample size: 1 Lot, 3ea/ Lot
- Test Reference: AEC Q100-002

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	0 Fails, 2KV(Class 2)	PASS

6.2 ESD Test (Charged Device Model, CDM)

Purpose:

The purpose is to establish a reliable and repeatable procedure for determiningthe CDM ESD sensitivity for electronic devices. This model is for characterizing the susceptibility of an electronicdevice to damage from electrostatic discharge (ESD). The model is an alternative to the human- body model (HBM).

Test Condition(s):

- <750V corner pins, 500V all other pins
- Sample size: 1 Lot, 3ea/ Lot
- Test Reference: AEC Q100-011

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	0 Fails, 750 corner pins, 500V all other pins (Class 4B)	Pass

Criteria: Acc/Rej = 0/1

6.3 Latch-Up Test (LU)

Purpose:

The latch-up test is to evaluate the immunity of semiconductor devices (mainly CMOS devices) to"latch-up" that is a temporary short-circuiting between the power source and the ground causedby electrical noise coming from I/O and power supply pins of a device through two parasitic bipolar structures before a power supply is removed.

Test Condition(s):

- Tigger Current : 100mA~ 200mA(±); Step: 50V(±)
- Over Voltage Test: VDD 2V(±) with Limit: 500mA; VCCQ3V(+) with Limit: 500mA; VCC 5.5V(+) with Limit: 500mA
- Test Temperature: room temp. and 85°C
- Sample size: 1 Lot, 6ea/ Lot
- Test Reference: AEC Q100-004

Test Result:

Product	Test Criteria	Result
eMMC 153-balls	0 Fails	Pass

Criteria: Acc/Rej = 0/1

7 CONCLUSION

All of samples passed the functional, electrical characteristic and cosmetic check before, during and after each reliability test.