



**SMART**semi<sup>TM</sup>

# **SMARTsemi** **Memory IC Datasheet**

**Industrial Grade eMMC 153b**

**Preliminary Release**

*April 2023  
Rev 0.1*

## REVISION HISTORY

Date	Revision	Section(s)	Description
April 2023	0.1	All	Preliminary Release



### ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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## 1 GENERAL DESCRIPTION

### 1.1 Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, Global wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMARTsemi's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high-density mass storage solution.

## 1.2 Features

- Industrial Standard Interface
  - JEDEC / eMMC Standard Version 5.1 Compliant
- eMMC 5.1 Enhanced Features
  - 12-signal interface (including CMD, CLK, DS, DAT[7:0], and RST\_n)
  - Programmable bus width: 1-bit, 4-bit, and 8-bit
  - Supports HS400 high mode
  - Up to 200MHz clock frequency
  - Supports eMMC Field firmware update (FFU)
  - Supports eMMC production state awareness (PSA)
  - High-speed, Dual Data Rate Boot support
  - Supports Boot and Alternative Boot Mode
  - Replay Protected Memory Block (RPMB)
  - Trim, Sanitize, Discard, Secure Erase
  - High Priority Interrupt (HPI)
  - Background Operations, Garbage Collection and WearLeveling
  - Reliable Write
  - Supports Command Queuing
  - Supports Enhanced Strobe in HS400 Mode
  - Supports eMMC Background Operation
  - Supports Secure Removal Type
  - Supports Secure Write Protection
  - Supports Cache, Cache Barrier, Cache Flushing Report
  - Enhance techniques: Sleep Notification in power off notification, data tagging, packed commands, discard, sanitize, RTC (real time clock)
  - Enhanced Partition Attributes
- LDPC ECC Engine
  - Support multiple parity size with 1KB based codeword
  - Support low-power decoding mode and high-correction capability decoding with soft information.
- Supply Voltage
  - eMMC Interface Power (VCCQ): 1.70-1.95V or 2.7-3.6V<sup>1</sup>
  - NAND Memory Power (VDD): 2.7-3.6V
- Multiple Densities and Packages
  - 153-ball standard BGA packages
  - REACH and RoHS Compliant
- Operating Temperature
  - Industrial Grade: -40°C ~ +85°C

Note: <sup>1</sup> HS200 and HS400 mode are not supported when VCCQ is in 2.7-3.6V.

## 2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

### 2.1 Performance

**Table 1: Performance Table**

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8 GB	335	110	4900	1400
16 GB	335	110	4900	1400
32 GB	335	110	4900	1400
64 GB	335	110	4900	1400
128 GB	335	170	4900	1400

(1) Test condition: Testmetrix VTESA-4100E; bus in x8 I/O mode.

### 2.2 Power Consumption

**Table 2: Current Consumption**

Condition1		ICC/ICCQ (Typical)					Units
		8GB (native)	16GB (native)	32GB (native)	64GB (native)	128GB (native)	
Write	DDR52	16/45	17/48	17/45	18/48	18/48	mA
	HS200	52/66	54/69	64/70	65/70	68/70	mA
	HS400	59/69	63/72	65/75	68/75	70/78	mA
Read	DDR52	13/63	14/65	14/67	15/68	25/70	mA
	HS200	22/68	24/71	24/72	24/72	32/75	mA
	HS400	25/73	25/76	25/77	30/77	35/77	mA
Sleep current		80	80	80	80	80	µA
Standby		28/80	28/80	28/80	28/80	28/80	µA

(1) The testing result is measured by TestMetrix VTE-4100.

## 2.3 Data Reliability

- Wear Leveling:** Efficient algorithms prolong the life of NAND by monitoring the cells in the device.
- ECC:** Utilize LDPC ECC to provide correction of user data.
- Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

## 2.4 Failure Rate

**Table 3: Failure Rate**

Failure Rate <sup>(1)</sup>	All capacities
FIT @55°C	TBD

(1) The FIT data generated from high temperature experiment: Sample size = 77ea, 1 Lot.

## 2.5 Environmental Conditions

**Table 4: Environmental Conditions and Test Conditions**

Parameter	Value
Operating Temperature – Industrial Grade	-40°C to 85°C
Storage Temperature	-40°C to 85°C

## 2.6 Endurance<sup>1</sup>

**Table 5: Reliability Characteristics**

Item	Value	
Data Retention (@ 40°C)	3 years when 90% life remaining	
	1 year when 10% life remaining	
100% Sequential Workload	8GB	TBD
	16GB	TBD
	32GB	TBD
	64GB	TBD
	128GB	TBD

<sup>1</sup> Endurance is directly related to the User specific workload.

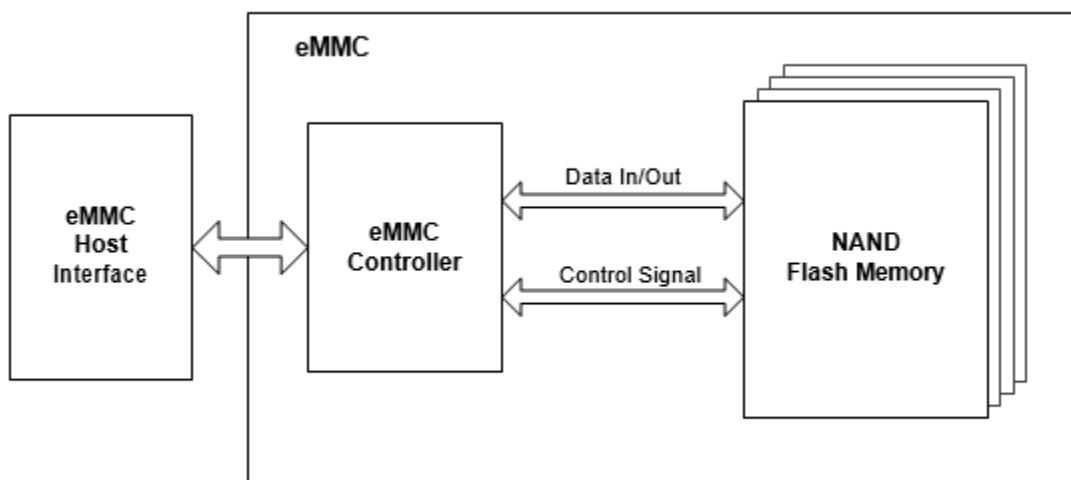


### 3 PRODUCT DESCRIPTION

The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

#### 3.1 Functional Block Diagram

Figure 1: eMMC Block Diagram



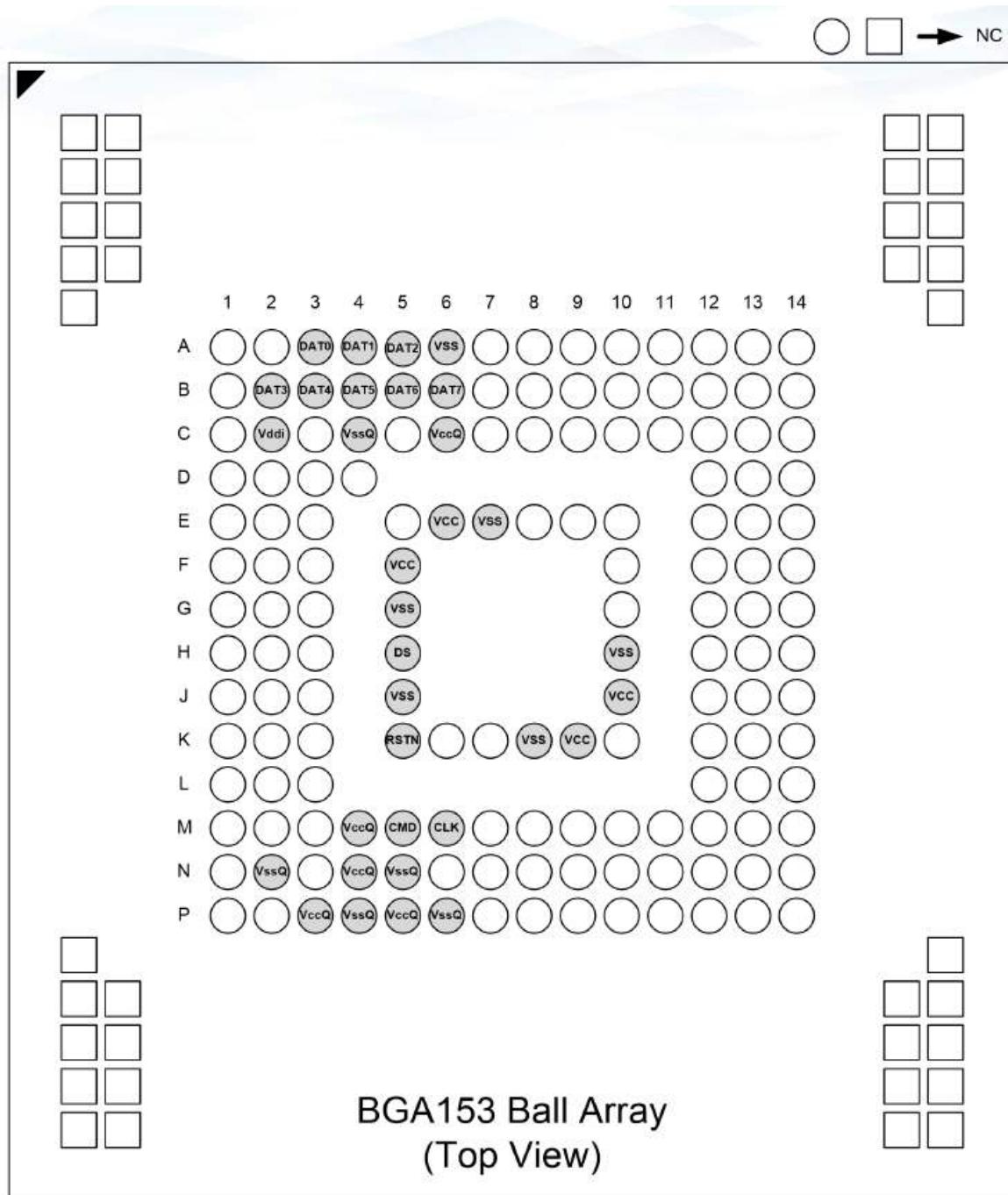


## 4 PACKAGE INFORMATION

### 4.1 Signal Interface

#### 4.1.1 eMMC Ball-out Diagram

Figure 2: 153-Ball Pin Assignments (Top View, Balls Down)\*



#### 4.1.2 Signal Descriptions

**Table 6: Signal Descriptions**

Table 6 contains the eMMC functional pins assignment.

Pin Number	Name						
A3	DAT0	C2	VDDi	J5	VSS	N4	VCCQ
A4	DAT1	C4	VSSQ	J10	VCC	N5	VSSQ
A5	DAT2	C6	VCCQ	K5	RSTN	P3	VCCQ
A6	VSS	E6	VCC	K8	VSS	P4	VSSQ
B2	DAT3	E7	VSS	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	VSSQ
B4	DAT5	G5	VSS	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	VSS	N2	VSSQ		

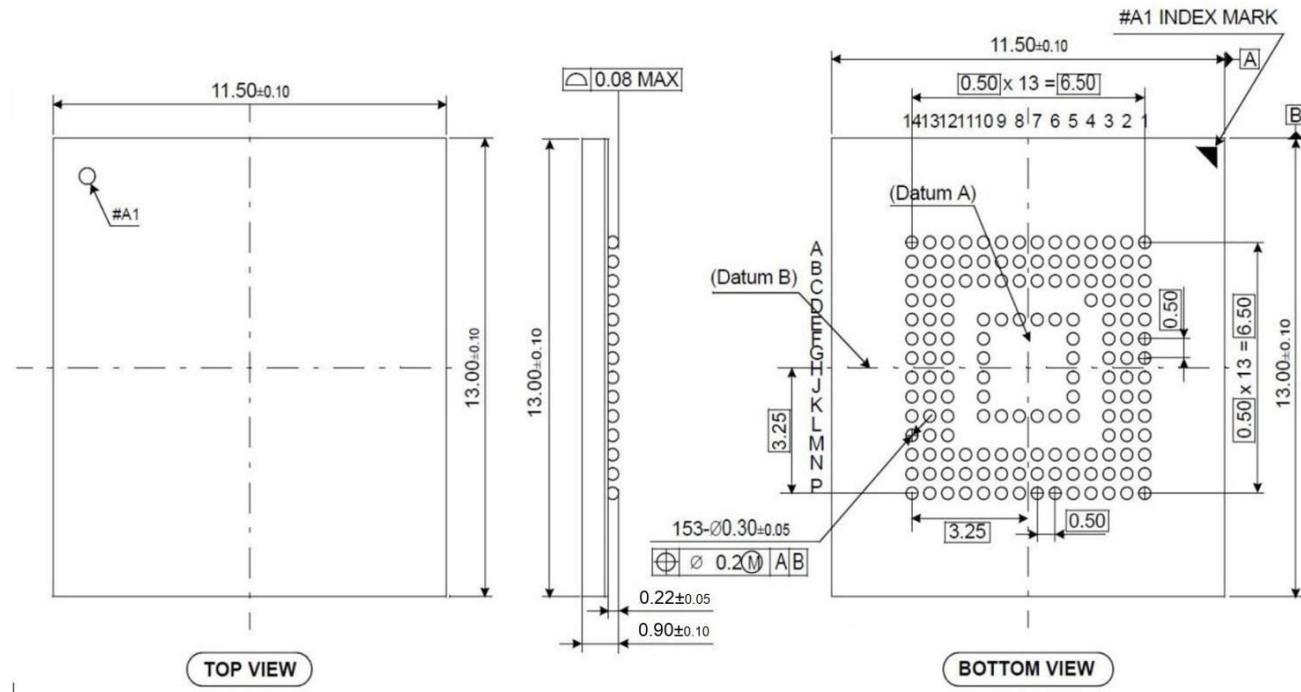
- CLK : Clock input
- DS: Data Strobe is generated from eMMC to host.
- In HS400 mode, read data and CRC response are synchronized with Data Strobe.
- CMD: A bidirectional signal used for device initialization and command transfers.
- Command operates in two modes, open-drain for initialization and push-pull for fast command transfer.
- DAT0-7: Bidirectional data channels. It operates in push-pull mode.
- RSTN : H/W reset signal pin
- VCC : Supply voltage for flash memory
- VCCQ : Supply voltage for memory controller
- VDDi : Internal power node to stabilize regulator output to controller core logics
- VSS : Ground connections
- NC: No Connection and left floating.



## 5 eMMC MECHANICAL SPECIFICATIONS

### 5.1 Package Dimensions

Figure 3: 153-Ball BGA Dimensions – 11.5 mm x 13 mm x 0.9 mm



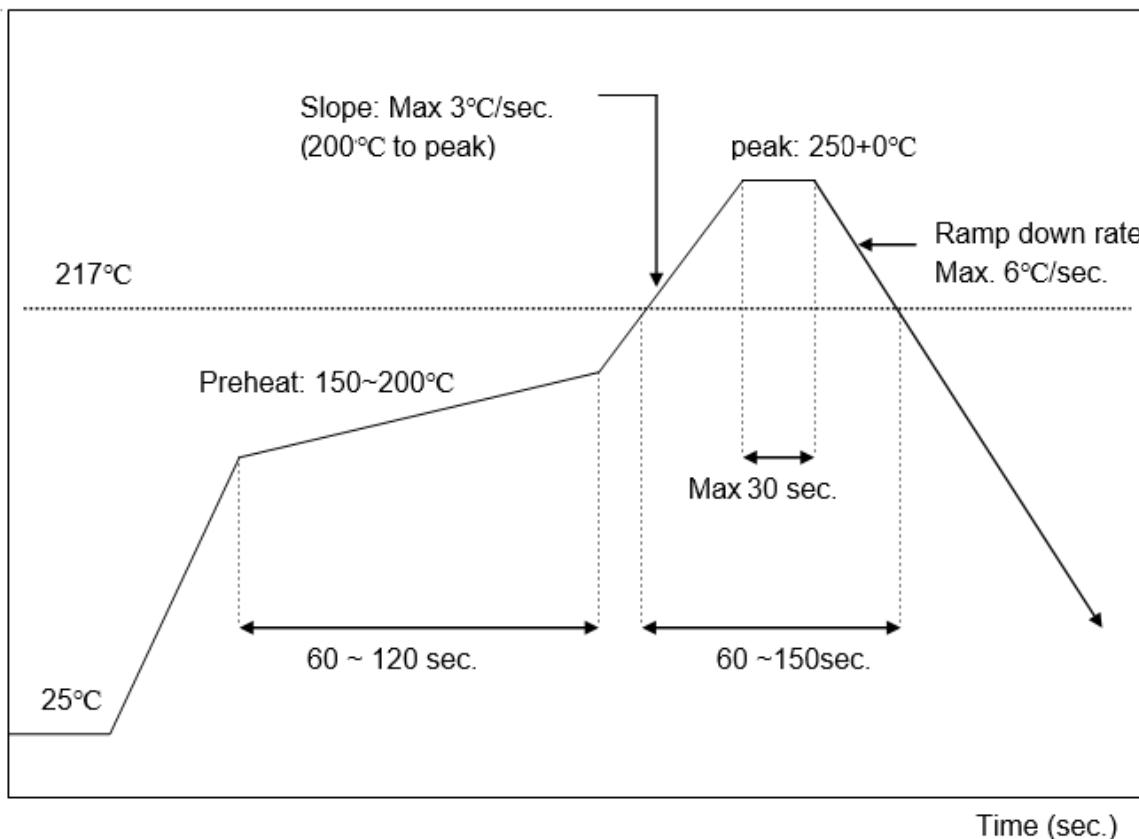


## 5.2 Recommended Reflow Profiles

Table 7: Recommended Reflow Profile

Reflow Parameters	Suggested Range
Specifications:	IPC/JEDEC J-STD-020E
Average ramp-up rate (200°C to peak):	3 °C/sec. max
Preheat:	150~200°C, 60~120 seconds
Temperature maintained above 217°C:	60~150 seconds
Time within 5°C of actual peak temperature:	255~260°C, 30 seconds
Peak temperature:	260+0°C
Ramp-down rate:	6°C/sec. max.
Time 25°C to peak temperature:	480 sec. max.

Figure 4: Recommended Reflow Profile





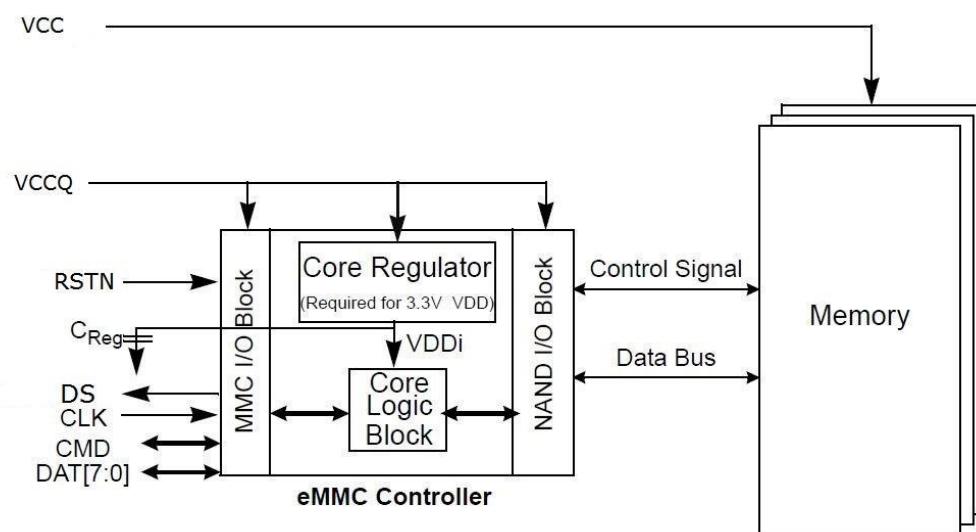
## 6 ELECTRICAL SPECIFICATION

### 6.1 Electrical Interface

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V<sub>CC</sub> is used for the NAND Flash device; V<sub>CCQ</sub> is used for the eMMC interface voltage.

**Figure 5: System Architecture**



### 6.2 DC Specifications

**Table 8: Power Requirements**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CCQ</sub> (Low)	1.7	1.95	V
	V <sub>CCQ</sub> (High)	2.7	3.6	V
	V <sub>CC</sub>	2.7	3.6	V
	V <sub>SS</sub> , V <sub>SSQ</sub>	-0.3	0.3	V



Figure 6: Recommended eMMC Connection

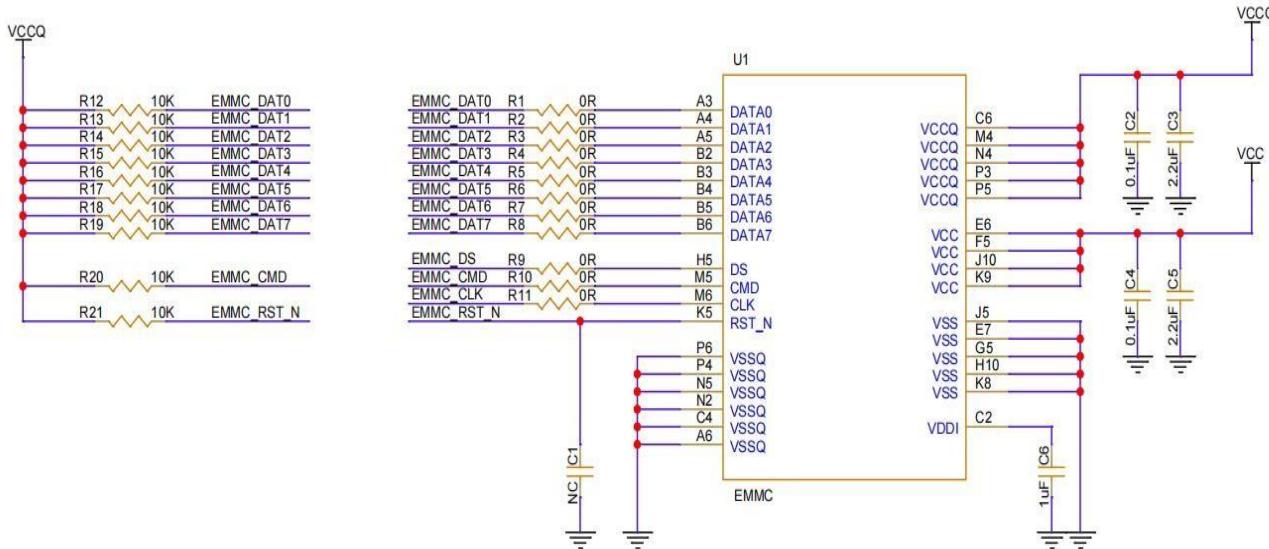


Table 9: Recommended Capacitor and Resistor

Parameter	Symbol	Recommended	Unit	Remark
Pull-up resistance for CMD	EMMC_CMD	4.7 to 100	kΩ	To prevent bus from floating
Pull-up resistance for DAT[7:0]	EMMC_DAT	10 to 100	kΩ	To prevent bus from floating
Pull-up resistance for RST_N	EMMC_RST_N	10	kΩ	
Series termination for CLK	EMMC_CLK	0 to 100	Ω	
Pull-down resistance for Data Strobe	EMMC_DS	10 to 100	kΩ	

## Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps connected with VCC/VCCQ and VSS as closely as possible.
- Recommended Value and Quantity:  
VCCQ: More than 0.1 μF x 1, 2.2 μF x 1  
VCC: More than 0.1 μF x 1 and 2.2 μF x 1  
VDDI: More than 1 μF x 1

## 7 REGISTER

The registers used in the SMART eMMC are shown in the table below. These registers are described in the sections that follow:

**Table 10: Supported Device Registers**

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

### 7.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

**Table 11: CID Register Field Parameters**

Name	Filed	Width (Bits)	CID Bits	SMART CID Value	
Manufacturer ID	MID	8	[127:120]	F6h	
Card BGA	CBX	2	[113:112]	01h	
OEM/Application ID	OID	8	[111:104]	00h	
Product name	PNM(1)	48	[103:56]	8GB	8GY1AΔ
				16GB	AGY1AΔ
				32GB	BGY1AΔ
				64GB	CGY1AΔ
				128GB	DGY1AΔ
Product revision	PRV	8	[55:48]	10h	
Product serial number	PSN	32	[47:16]	--(2)	
Manufacturing date	MDT	8	[15:8]	--(3)	
Calculated CRC	CRC	7	[7:1]	--(4)	

(1) The product name uses ASCII code and 'Δ' is a space (0x20)

(2) Unique for each device. 32-bit unsigned binary integer.

(3) 2 hex digits for device manufacturing month and year.

(4) CRC for CID register. Different for each device

## 7.2 OCR Register

The card identification (OCR) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

**Table 12: OCR Register Field Definitions**

VDD Voltage Windows	Width (Bits)	OCR Bits	OCR Value
Access mode	2	[30:29]	2h
VDD: 2.7 - 3.6 range	9	[23:15]	1FFh
VDD: 2.0 - 2.6 range	7	[14:8]	00h
VDD: 1.7 - 1.95 range	1	[7]	1h

## 7.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM\_CSD (CMD27) command.

**Table 13: CSD Register Field Parameters**

Name	Field	Width (Bits)	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	[127:126]	0x03
System specification version	SPEC_VERS	4	[125:122]	0x04
Reserved	-	2	[121:120]	--
Data read access time 1	TAAC	8	[119:112]	0x27
Data read access time 2 in CLK cycles (NSAC x 100)	NSAC	8	[111:104]	0x01
Maximum bus clock frequency	TRAN_SPEED	8	[103:96]	0x32
Device command classes	CCC	12	[95:84]	0xF5
Maximum read data block length	READ_BL_LEN	4	[83:80]	0x9
Partial blocks for reads supported	READ_BL_PARTIAL	1	[79]	0x0
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0x0
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0x0
DSR implemented	DSR_IMP	1	[76]	0x0



Name	Field	Width (Bits)	CSD Bits	CSD Value
Reserved	-	2	[75:74]	--
Device size	C-SIZE	12	[73:62]	0xFFFF
Maximum read current as VDD,min	VDD_R_CURR_MIN	3	[61:59]	0x7
Maximum read current as VDD,max	VDD_R_CURR_MAX	3	[58:56]	0x7
Maximum write current as VDD,min	VDD_W_CURR_MIN	3	[55:53]	0x7
Maximum write current as VDD,max	VDD_W_CURR_MAX	3	[52:50]	0x7
Device size multiplier	C-SIZE_MULT	3	[49:47]	0x7
Erase group size	ERASE_GRP_SIZE	5	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	[36:32]	8GB
				16GB
				32GB
				64GB
				128GB
				0x1F
Write protect group enable	WP_GRP_ENABLE	1	[31]	0x1
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0x0
Write-speed factor	R2W_FACTOR	3	[28:26]	0x2
Maximum write data block length	WRITE_BL_LEN	4	[25:22]	0x9
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0x0
Reserved	-	4	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	[16]	0x0
File-format group	FILE_FORMAT_GRP	1	[15]	0x0
Copy flag (OTP)	COPY	1	[14]	0x1
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0x0
Temporary write protection	TEMP_WRITE_PROTECT	1	[12]	0x0
File format	FILE_FORMAT	2	[11:10]	0x0
ECC code	ECC	2	[9:8]	0x0
CRC	CRC	7	[7:1]	0x00
Not used; always 1	-	1	[0]	0x1



## 7.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

**Table 14: ECSD Register Field Parameters**

Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Reserved	--	6	--	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported command sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x20
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x20
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x00
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x78
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x01
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES	1	R	[493]	0x01
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x17
FFU Argument	FFU_ARG	4	R	[490:487]	0xFFFFFFF0
Reserved	--	181	--	[486:306]	0x01
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x00
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	Variable
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	Variable
Pre EOL information	PRE_EOL_INFO	1	R	[267]	Variable



Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x40
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x40
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x07
Device Version	Device version	8GB	R	[263:262]	0x4205
		16GB			0x4305
		32GB			0x4405
		64GB			
Firmware version	FIRMWARE_VERSION	128GB			
		8	R	[261:254]	Variable <sup>(1)</sup>
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x400
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x10
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x64
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x0A
Reserved	--	1	--	[240]	0x01
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200 MHz at 1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200 MHz at 1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved	--	1	--	[233]	--
TRIM multiplier	TRIM_MULT	1	R	[232]	0x02
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55



Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
SECURE ERASE multiplier	SEC_ERASE_MULT	8GB 16GB 32GB 64GB	R	[230]	0x19
		128GB			0x32
SECURE TRIM multiplier	SEC_TRIM_MULT	1	R	[229]	0x0A
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved	--	1	--	[227]	--
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x06
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x05
Reliable write-sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	8GB 16GB 32GB 64GB	R	[221]	0x10
		128GB			0x20
Sleep current (Vcc)	S_C_VCC	1	R	[220]	0x07
Sleep current (Vccq)	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x17
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x12
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x0C
Sector count	SEC-COUNT	8GB	R	[215:212]	0xE8C000
		16GB			0x1D1C000
		32GB			0x3A3C000
		64GB			0x7478000
		128GB			0xE8F0000
Reserved	--	1	--	[211]	0x01
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x00



Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved	--	1	--	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0xA
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x0A
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card type	CARD_TYPE	1	R	[196]	0x57
Reserved	--	1	--	[195]	--
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	--	1	--	[193]	--
Extended CSD revision	EXT_CSD_REV	1	--	[192]	0x08
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	--	1	--	[190]	--
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	--	1	--	[188]	--
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	--	1	--	[186]	--
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved	--	1	--	[184]	0x01
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved	--	1	--	[182]	--
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved	--	1	--	[180]	--



Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved	--	1	--	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	0x00
Reserved	--	1	-	[172]	--
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	--	1	--	[170]	--
Firmware configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x15
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
Hardware reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT	1	R/W/E, R/W/E_P	[160]	0x07
Maximum enhanced area size	MAX_ENH_SIZE_MULT	8GB	3	[159:157]	0x136
		16GB			0x26D
		32GB			0x4DA
		64GB			0x9B4
		128GB			0x9B4
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00

Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Partitioning setting	PARTITIONING_SETTING-COMPLETED	1	R/W	[155]	0x00
General-purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved	-	1	-	[135]	--
Bad block management mode	SEC_BAD_BLK_MGMT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPOR	1	R	[130]	0x01
Reserved	-	2	-	[129:128]	--
Vendor specific fields	VENDOR_SPECIFIC_NFIELD	64	<vs>	[127:64]	0x00
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x01
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0xA
Class 6 command control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00



Name	Field	Size (Bytes)	Cell Type <sup>(1)</sup>	ECSD Bytes	ECSD Values
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved	-	2	-	[28:27]	--
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DA TASIZE	8GB	R	[21:18]	0x1335555
		16GB			0x266AAAA
		32GB			0x4DAAAAA
		64GB			
Product state awareness enablement	PRODUCT_STATE_AWARENESS_E NABLEMENT	128GB	R/W/E & R	[17]	0x01
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x3B
Reserved	-	16	-	[15:0]	--

(1) Note: FIRMWARE\_VERSION depends on capacity.



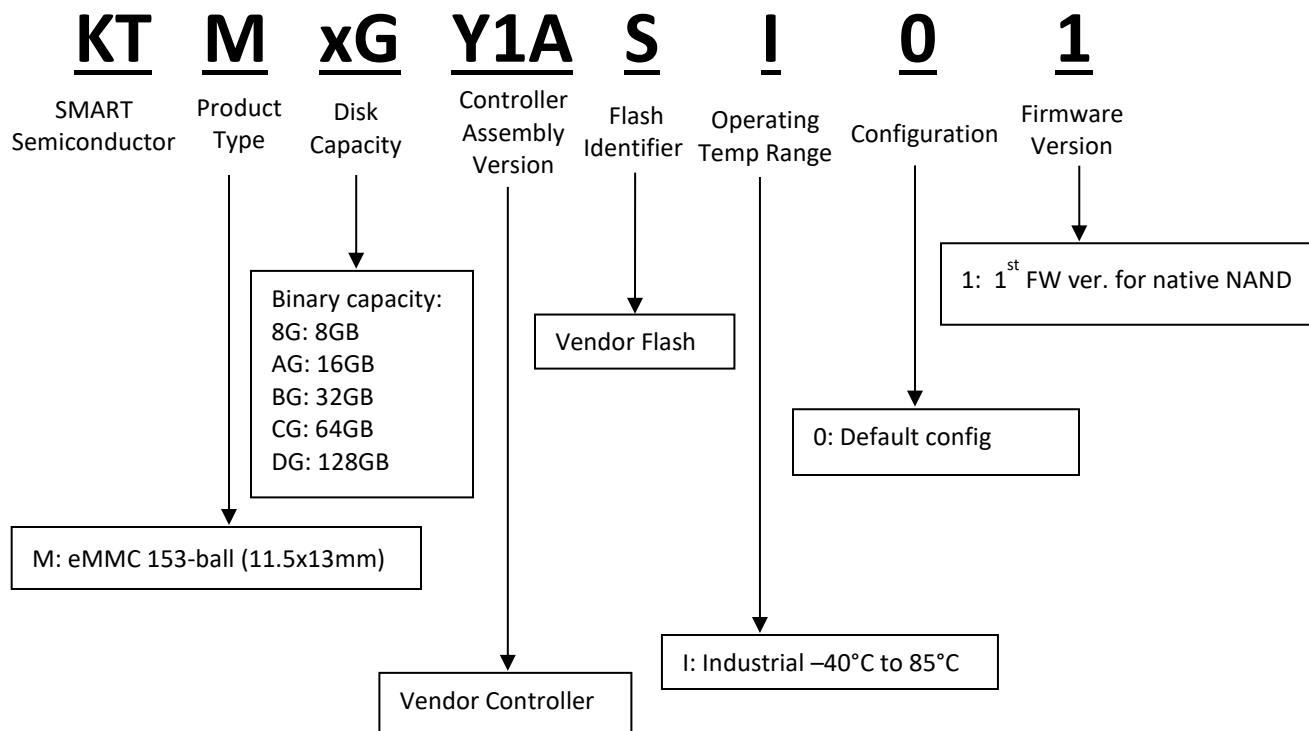
## 8 PART NUMBERS

Table 15: Part Numbering Information

Capacity	Part Number
8GB	KTM8GY1ASI01
16GB	KTMAGY1ASI01
32GB	KTMBGY1ASI01
64GB	KTMCGY1ASI01
128GB	KTMDGY1ASI01



## 8.1 Part Number Decoder



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