SMARTsemi
Memory Card Datasheet

Industrial Grade SD Card

September 2023
Rev 2.0

REVISION HISTORY

Date	Revision	Section(s)	Description
April 2023	0.1	All	Preliminary Release
August 2023	1.0	All	Initial Release
September 2023	2.0	Registers	Update Registers information

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1   GENERAL DESCRIPTION

1.1 Overview

SMARTsemi's SD Memory Card product is specifically target at the needs of OEM markets such as networking, telecommunications and data communications. SMARTsemi's SD products are also a natural fit for mobile and embedded computing, medical, automotive and industrial applications.

SMARTsemi's SD products offer reliable, high performance operation in an industry standard ultrasonic welded SD housing. They are available in 8 GB to 128 GB capacities.

Incorporating on-board error detection and correction algorithms and static and dynamic wear leveling techniques insure SMARTsemi's SD products provide years of reliable operation.

SMARTsemi has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMARTsemi engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

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1.2 Features

- **Form Factor:** SD Memory card
- **Capacity:**
  - MLC: 8 GB
  - pSLC: 16GB
  - TLC: 32GB/64GB/128GB
- **The command list supports s [Part 1 Physical Layer Specification Ver6.10 Final] definitions**
- **Supports SD SPI Mode**
- **Support File system specification version 3.0**
- **Supported Bus Speed Modes (using x4 bus width)**
  - **Default Speed Mode:** 3.3 V signaling, up to 25 MHz, up to 12.5 MB/s
  - **High Speed Mode:** 3.3 V signaling, up to 50 MHz, up to 25 MB/s
  - **SDR12:** 1.8 V signaling, up to 25 MHz, up to 12.5 MB/s
  - **SDR25:** 1.8 V signaling, up to 50 MHz, up to 25 MB/s
  - **SDR50:** 1.8 V signaling, up to100 MHz, up to 50 MB/s
  - **SDR104:** 1.8 V signaling, up to 208 MHz, up to 104 MB/s
  - **DDR50:** 1.8 V signaling, up to 50 MHz, up to 50 MB/s
  - NOTE: Timing varies between 1.8V and 3.3V signaling
- **Operating Temperature:**
  - **Industrial:** -40ºC to +85ºC
- **Input Power:** 2.7 V – 3.6 V
- **Dimension**s: 32 mm(L) x 24 mm(W) x 2.1 mm(H)
- **ESD protection:** +4 kV/-4 kV in contact pads

1.3 Unique Features

- Implements Static and Dynamic Wear Leveling for longer life
- Device health information (endurance life ratio and good block ratio) is available via specific utility (Application Note available upon request)
- Copyright Protection Mechanism: compliant to the highest security of SDMI Standard
- Supports CPRM (Content Protection for Recordable Media) for recorded content
- Password Protection of cards (optional)
- Provides a mechanical switch for Write Protection
- Built-in write protection features (permanent and temporary)
- RoHS compliant and Low Halogen

2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Table

Drive	Configuration	Sequential Read (MB/s)	Sequential Write (MB/s)
8GB	SDR104 (UHS-I, 1.8V, 208MHz)	95	35
16GB		100	85
32GB		100	15
64GB		100	50
128GB		100	85

Note: Performance measured using Testmetrix VTE-4100.

2.2 Power Consumption

Table 2: Current Consumption

Parameter	8GB	16GB	32GB	64GB	128GB	Unit
Read Current	120	100	100	105	105	(RMS) mA
Write Current	85	105	90	110	115	(RMS) mA
Standby Current	1000	1000	1000	1000	1000	(RMS) µA

Note**:** Current measured with scope (average value), under SDR104 mode operation.

2.3 Data Reliability

Table 3: Reliability and Endurance

Item			Value
Mean Time Between Failures (MTBF) (@ 25˚C)			> 3 Million hours
Data Reliability			< 1 Non-Recoverable Error in 10^{14} bits read
Data Retention (@ 40˚C)			10 years > 90% life remaining
			1 year < 10% life remaining
Endurance[1]		8GB	23 TBW
		16GB	460 TBW
		32GB	91 TBW
		64GB	183 TBW
		128GB	366 TBW

(1) Sequential write.

- **Static & Dynamic Wear Leveling:** This feature eliminates overstressing Flash media by spreading the data writes across all Flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.

- **ECC:** To detect and correct errors occur during Read process, ensure data been read correctly. As well as protect data from corruption.

- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of Flash media and replaces them with new ones from the spare pool.

2.4 Environmental Conditions

Table 4: Environmental Conditions and Test Conditions

Parameter	Value
Operating Temperature – Industrial Grade	-40°C to 85°C
Storage Temperature	-40°C to 85°C

3   PRODUCT DESCRIPTION

SMARTsemi's SD Memory Card product line is offered with an advanced 9-pin connector. It contains a controller and at least one Flash memory device. The on-board controller interfaces with a SD Card Host allowing data to be written to and read from the Flash memory device(s).

3.1 Functional Block Diagram

Figure 1: SD Block Diagram
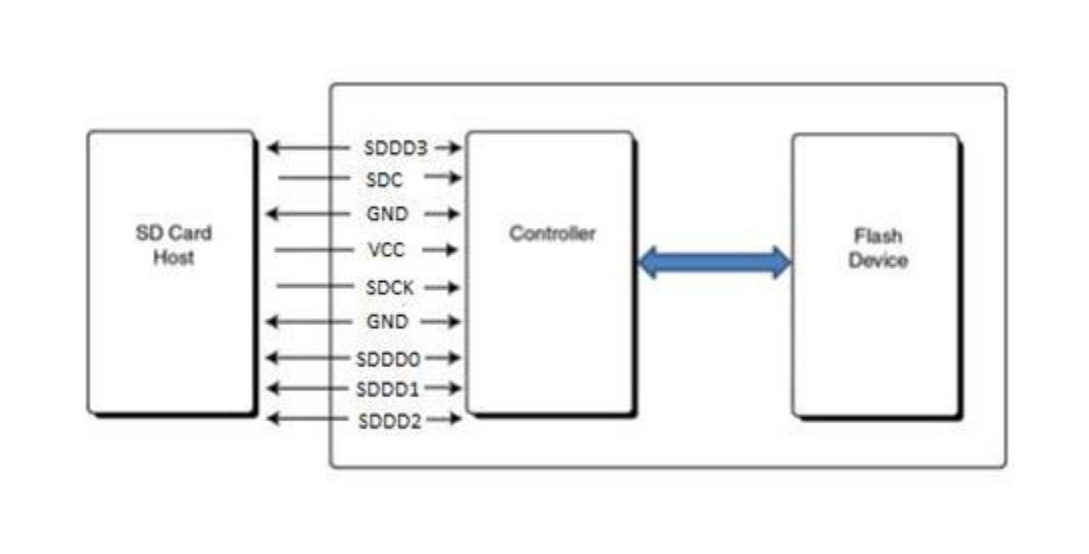
4   MECHANICAL SPECIFICATIONS

4.1 Mechanical Dimensions

Figure 2: SD Dimensions – (in mm)
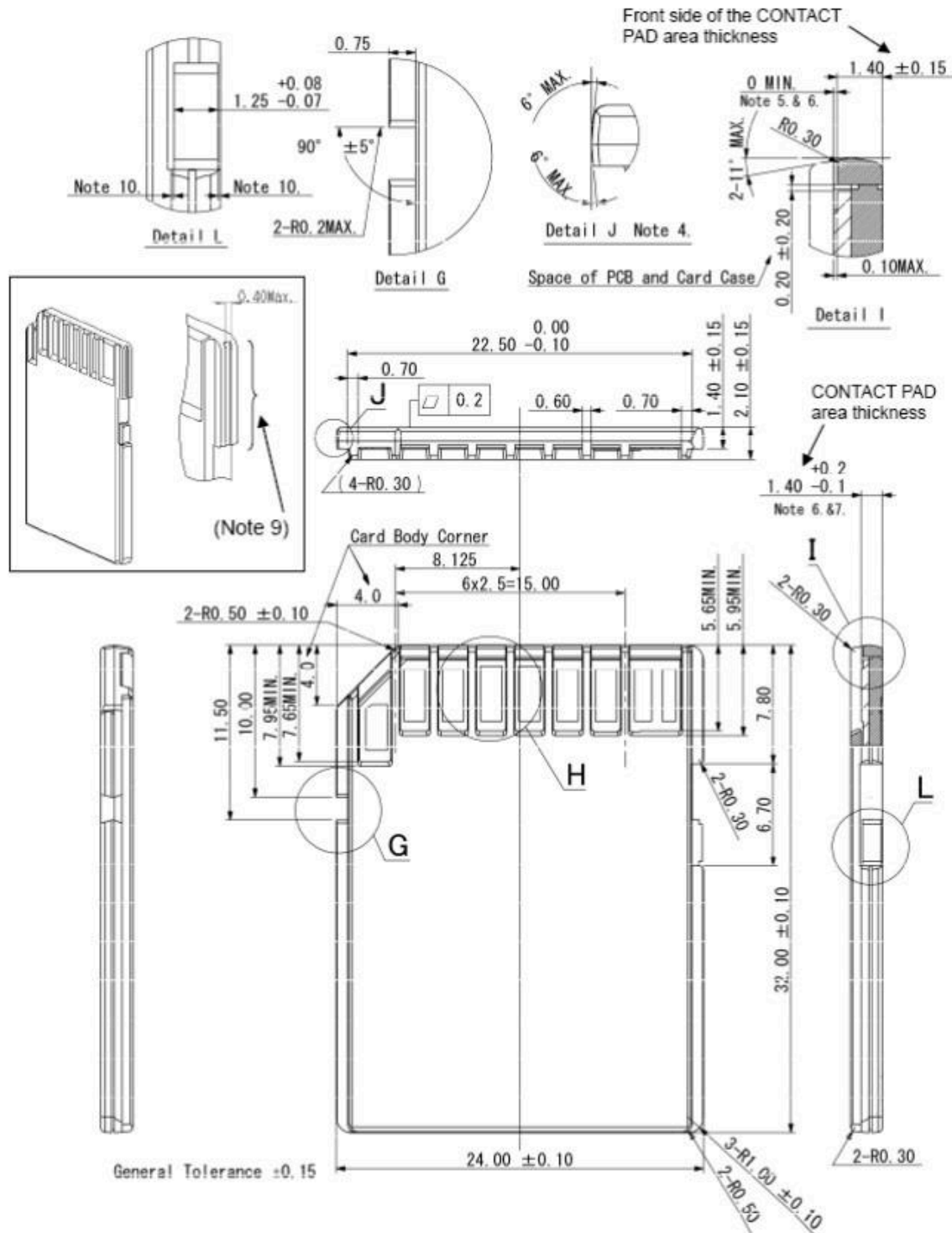
4.2   Physical Characteristics

Table 5: Physical Characteristics

Parameter	Value
Length	32.0 mm [1.26 in]
Width	24.0 mm [0.95 in]
Height	2.1 mm [0.08 in]
Weight (max)	2.0 g [0.07 oz]

4.3   Housing

Below are examples of the standard housing for the SMARTsemi SD card.

Figure 3: SD housing – Industrial
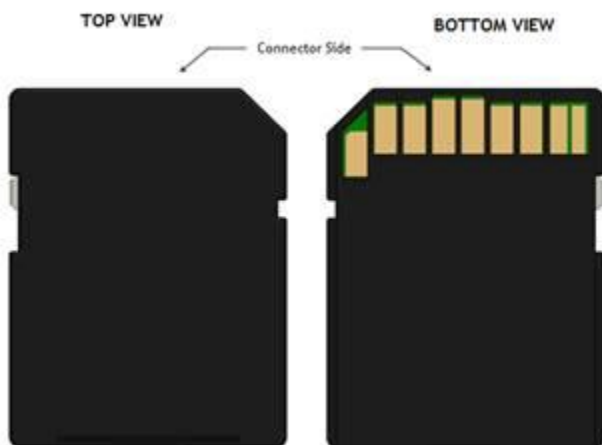
5   ELECTRICAL SPECIFICATION

5.1 Electrical Interface

The SMARTsemi SD Memory Cards are fully compliant with the SD specification (V3.01). The following table describes the I/O signals of the card. Signals whose source is the Host are designated as inputs (I), while signals that the SD Card sources are outputs (O). Bi-directional signals are designated as Input/output (I/O).

Table 6: Pinout Assignments and Pin Types

Pin	Signal Name	Signal Type	Signal Description
1	SDDD3	I/O,PP	SD Interface Bus [3]
2	SDC	PP	SD Command Line
3	GND	S	Ground
4	VCC	S	Power Supply for SD Interface
5	SDCK	I	SD Synchronous Clock Input
6	GND	S	Ground
7	SDDD0	I/O,PP	SD Interface Bus [0]
8	SDDD1	I/O,PP	SD Interface Bus [1]
9	SDDD2	I/O,PP	SD Interface Bus [2]

Type Key: S=power supply; I=input; O=output using push-pull drivers; PP=I/O using push-pull drivers

5.2   Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings [1]

Parameter	Minimum Value	Maximum Value	Unit
3.3 V Supply Voltage	-0.3	3.6	V
3.3 V Input Voltage	GND - 0.3	VCC + 0.3	V
Operating Current	-	800	mA
Operating Temperature – (Industrial)	-40	+85	^{o}C
Storage Temperature – (Industrial)	-40	+85	^{o}C

[1]Stress beyond the Absolute Maximum Rating conditions may result in permanent damage to the device. These are stress ratings only and functional operation should be restricted to those indicated in the operational sections of this specification. Exposure to conditions beyond recommended, up to and including the Absolute Maximum Rating conditions, for extended periods may affect device reliability.

6 DC CHARACTERISTICS

6.1 Bus Operation Conditions for 3.3V Signaling

Table 8: Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	$0.75*V_{DD}$		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		$0.125*V_{DD}$	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	$0.625*V_{DD}$	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	$0.25*V_{DD}$	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 9: Peak Voltage and Leakage Current

Parameter	Min.	Max	Unit
Peak voltage on all lines	-0.3	V_{DD}+0.3	V
All Inputs			
Input Leakage Current	-10	10	µA
All Outputs			
Output Leakage Current	-10	10	µA

6.2 Bus Operation Conditions for 1.8V Signaling

Table 10: Threshold Level for 1.8 V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Supply Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH}=-2mA
Output Low Voltage	V_{OL}		0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

Table 11: Input Leakage Current for 1.8V Signaling

Parameter	Min.	Max	Unit	Remarks
Input Leakage Current	-2	2	µA	DAT3 pull-up is disconnected.

6.3   SD Memory Card Hardware Interface

Figure 4: Bus Circuitry Diagram
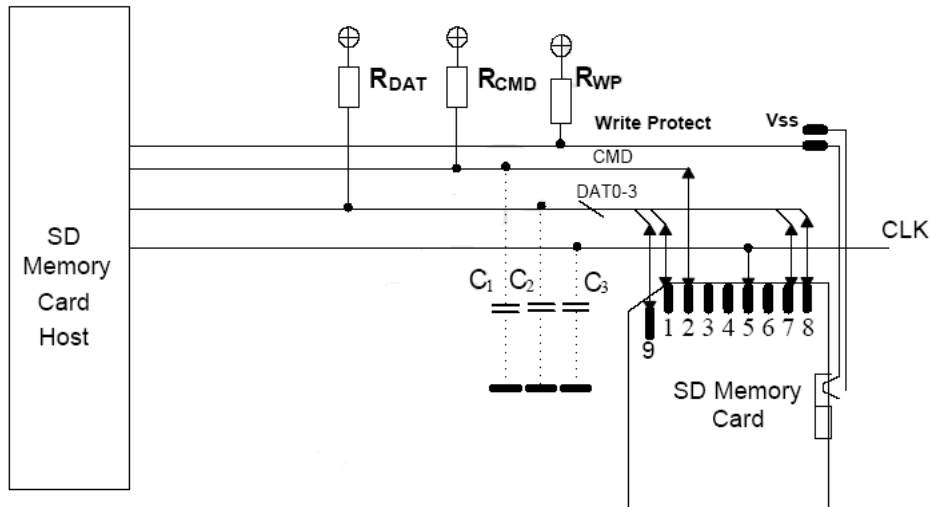
6.4   Bus Signal Line Loading (Recommended)

Table 12: Bus Signal Line Loading (Recommended)

Symbol	Parameter	Min	Max	Units	Remark
R_{CMD}	Pull-up Resistor for CMD Signal	10	100	kΩ	to prevent bus floating
R_{DAT}	Pull-up Resistor for DAT Signals	10	100	kΩ	to prevent bus floating
C_L	Total bus capacitance for each signal line		40	pF	1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF
C_{CARD}	Card Capacitance for each signal pin		10	pF	
-	Maximum signal line inductance		16	nH	
R_{DAT3}	Pull-up resistance inside card	10	90	kΩ	May be used for card detection
C_C	Capacity Connected to Power Line		5	μF	To prevent inrush current

7 AC CHARACTERISTICS

Figure 5: Bus Signal Level
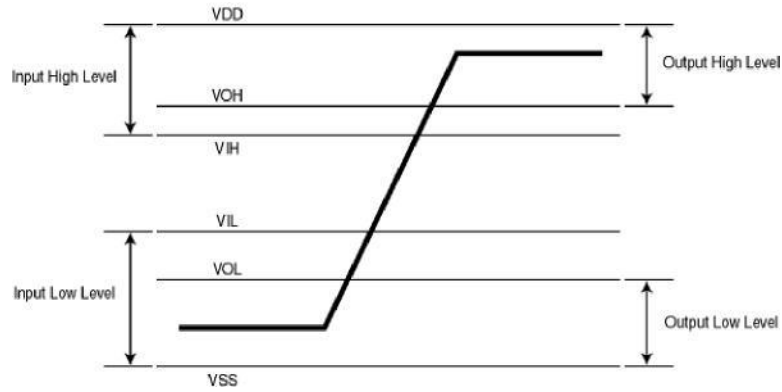
7.1 Interface Timing (Default Speed Mode)

Figure 6: Card Input Timing (Default Speed Mode)
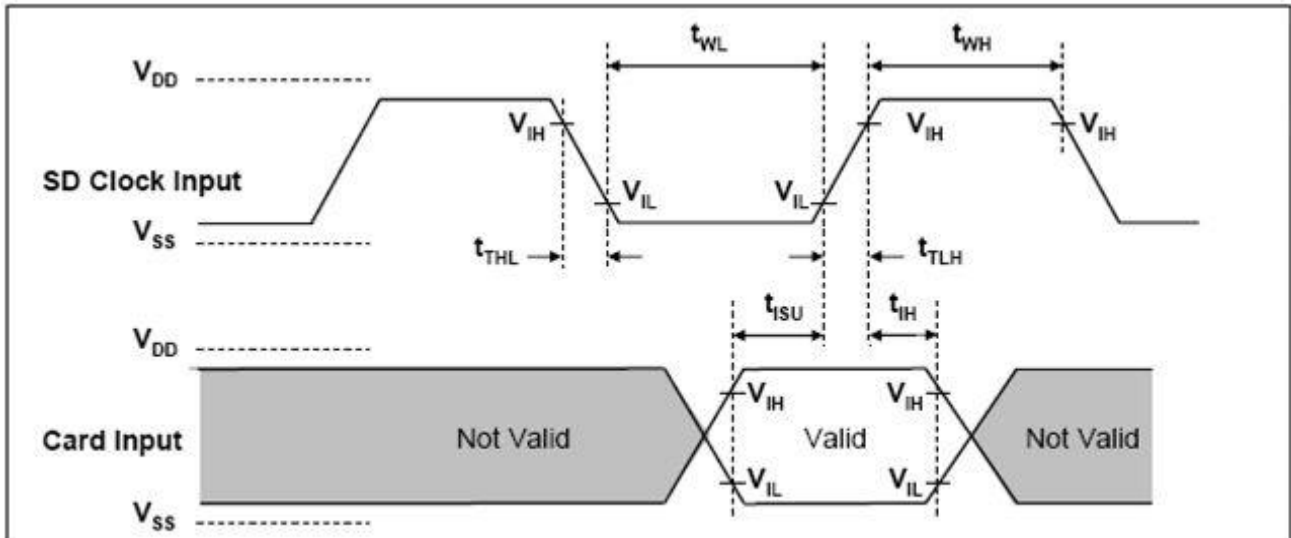
Figure 7: Card Output Timing (Default Mode)
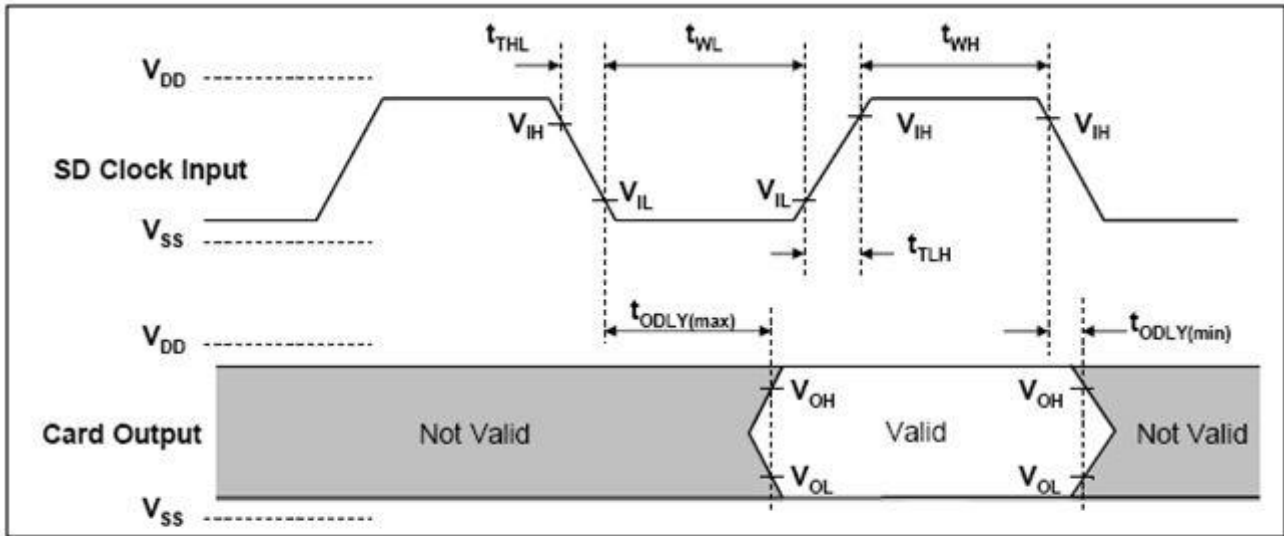
Table 13: Bus Timing (Default Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark [1]
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency data transfer mode	0	25	MHz	$C_{card} \leq 10$ pF
f_{OD}	Clock frequency Identification Mode	0[2]/100	400	kHz	
t_{WL}	Clock low time	10		ns	$C_{card} \leq 10$ pF
t_{WH}	Clock high time	10		ns	$C_{card} \leq 10$ pF
t_{TLH}	Clock rise time		10	ns	$C_{card} \leq 10$ pF
t_{THL}	Clock fall time		10	ns	$C_{card} \leq 10$ pF
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	5		ns	$C_{card} \leq 10$ pF
t_{IH}	Input hold time	5		ns	$C_{card} \leq 10$ pF
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output delay time during Data Transfer Mode	0	14	ns	$C_L \leq 40$ pF
t_{ODLY}	Output delay time during Data Identification mode	0	50	ns	$C_L \leq 40$ pF

1. Values are for 1 card.
2. 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

7.2 Interface Timing (High Speed Mode)

Figure 8: Input Timing (High Speed Mode)
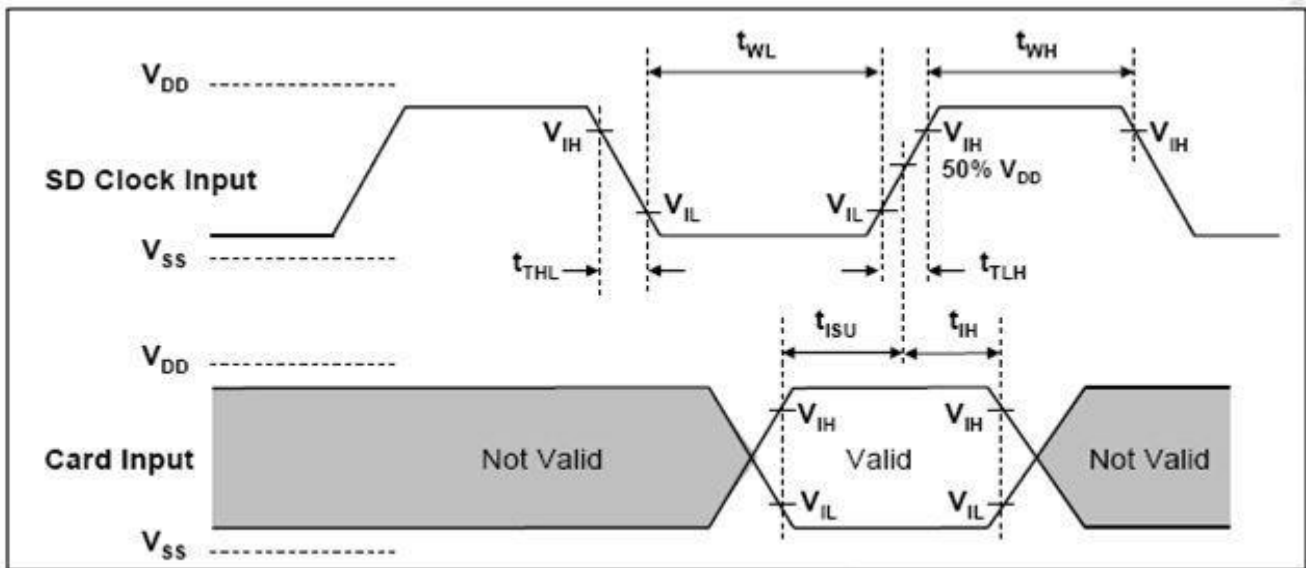
Figure 9: Output Timing (High Speed Mode)
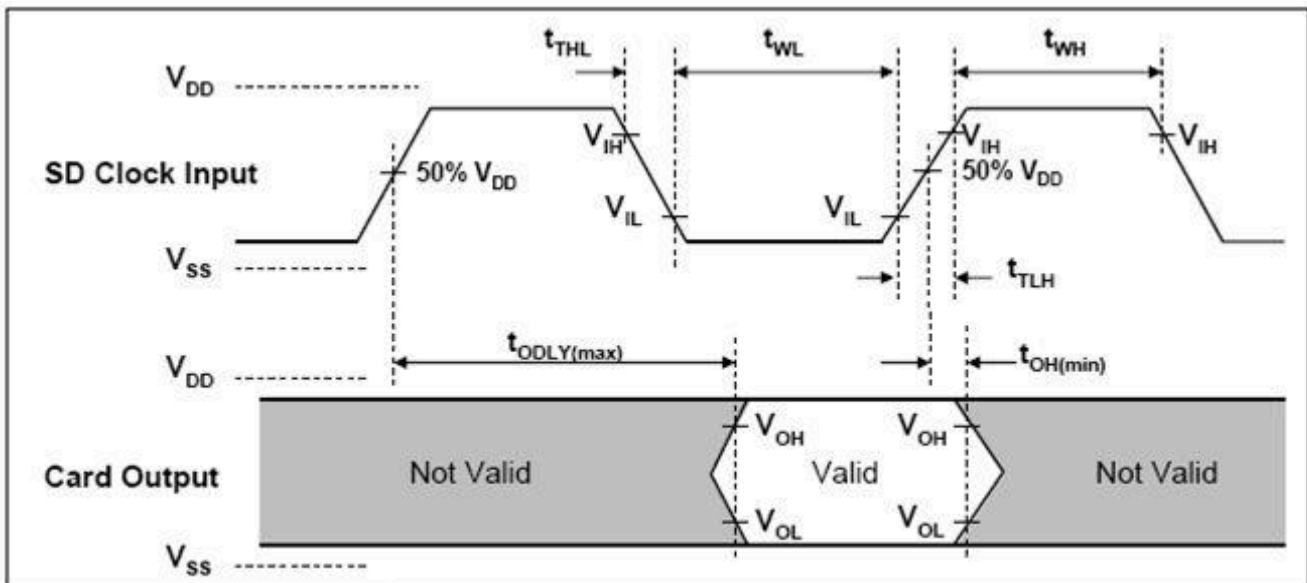
Table 14: Bus Timing (High Speed)

Symbol	Parameter	Min	Max	Unit	Remark[1]
**Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})**					
f_{PP}	Clock frequency data transfer mode	0	50	MHz	$C_{card} \leq 10$ pF
t_{WL}	Clock low time	7	-	ns	$C_{card} \leq 10$ pF
t_{WH}	Clock high time	7	-	ns	$C_{card} \leq 10$ pF
t_{TLH}	Clock rise time	-	3	ns	$C_{card} \leq 10$ pF
t_{THL}	Clock fall time	-	3	ns	$C_{card} \leq 10$ pF
**Inputs CMD, DAT (referenced to CLK)**					
t_{ISU}	Input setup time	6	-	ns	$C_{card} \leq 10$ pF
t_{IH}	Input hold time	2	-	ns	$C_{card} \leq 10$ pF
**Outputs CMD, DAT (referenced to CLK)**					
t_{ODLY}	Output delay time during Data Transfer Mode	-	14	ns	$C_L \leq 40$ pF
t_{OH}	Output Hold Time	2.5	-	ns	$C_L \leq 15$ pF
C_L	Total System Capacitance of each line	-	40	pF	$C_L \leq 15$ pF

1. In order to satisfy server timing, host shall drive only one card.

7.3 Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes)

Figure 10: Input Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max), Between rising edge, $V_{CT} = 0.975$V
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	t_{CR}, $t_{CF} < 0.96$ns (max.) at 208MHz, $C_{CARD} = 10$pF t_{CR}, $t_{CF} < 2.00$ns (max.) at 100MHz, $C_{CARD} = 10$pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Figure 11: Card Input Timing (SDR50 and SDR104)
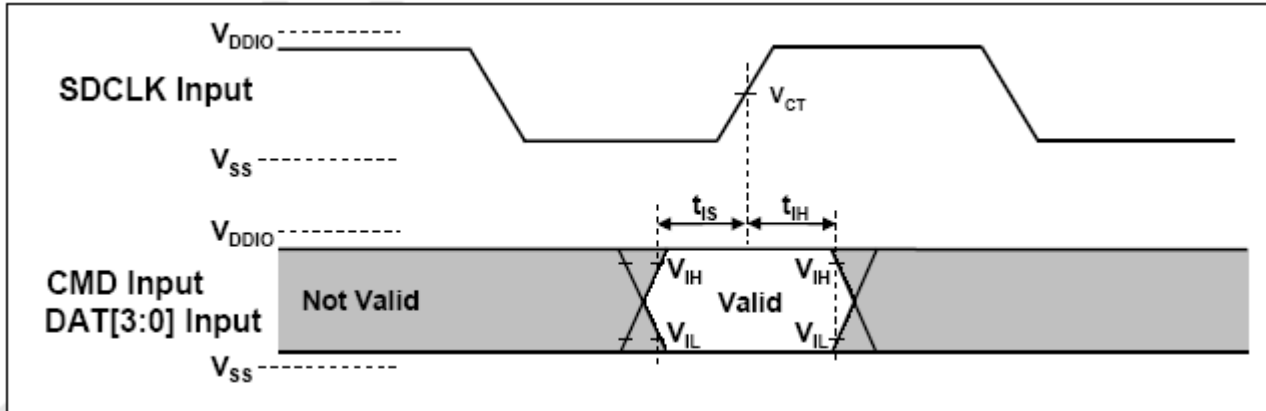
Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	Min	Max	Unit	SDR50 mode
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Figure 12: Output Timing - Fixed Data Window (SDR12, SD25 and SDR50)
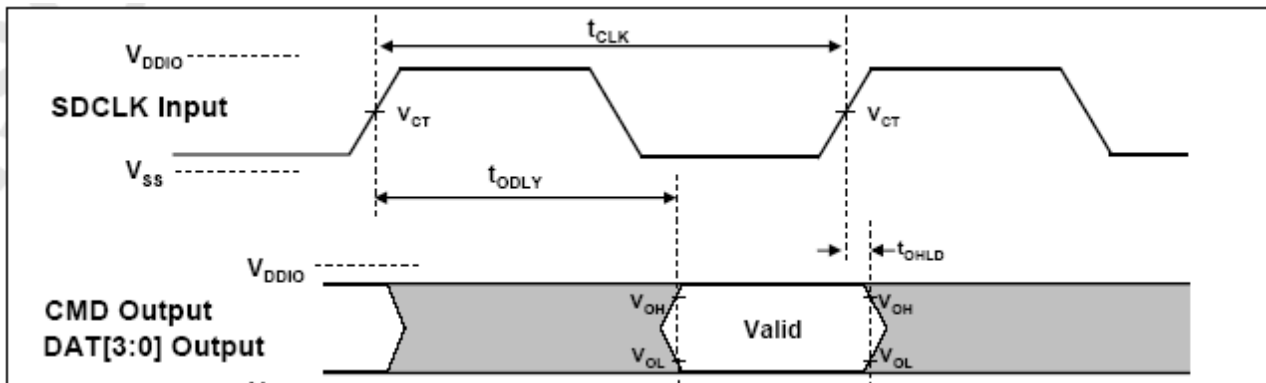
Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, CL=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

Figure 13: Output Timing - Variable Window (SDR104)
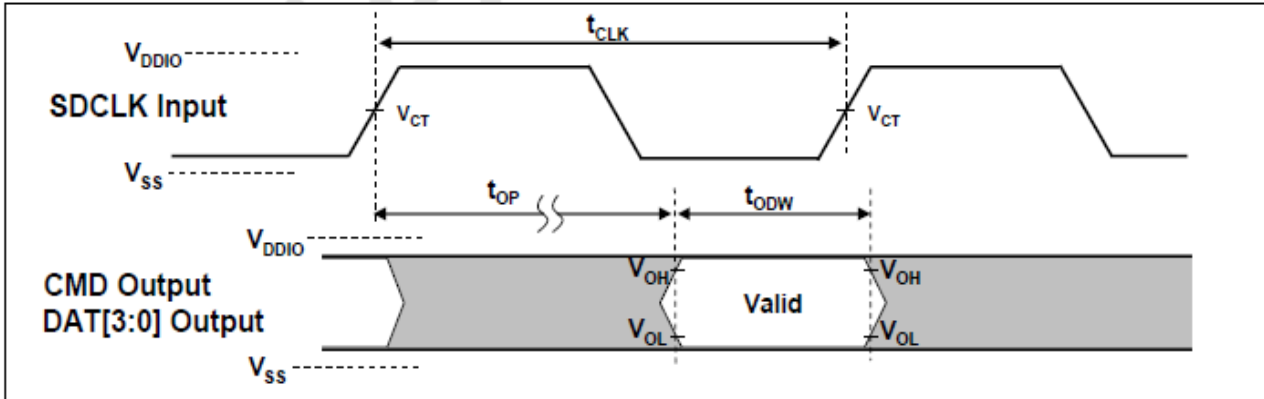
Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δ_{tOP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

7.4   Interface Timing (DDR50 Mode)

Figure 14: Interface Timing (DDR50 Mode)
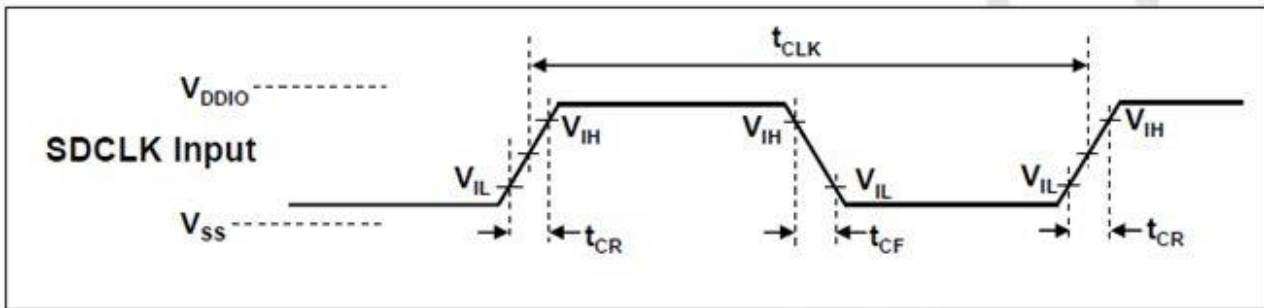
Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max) Between rising edge
t_{CR}, t_{CF}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (Max) at 50MHz, C_{CARD} = 10pF
Clock Duty	45	55	%	

Figure 15: DAT Inputs/Outputs Referenced to CLK in DDR50 Mode
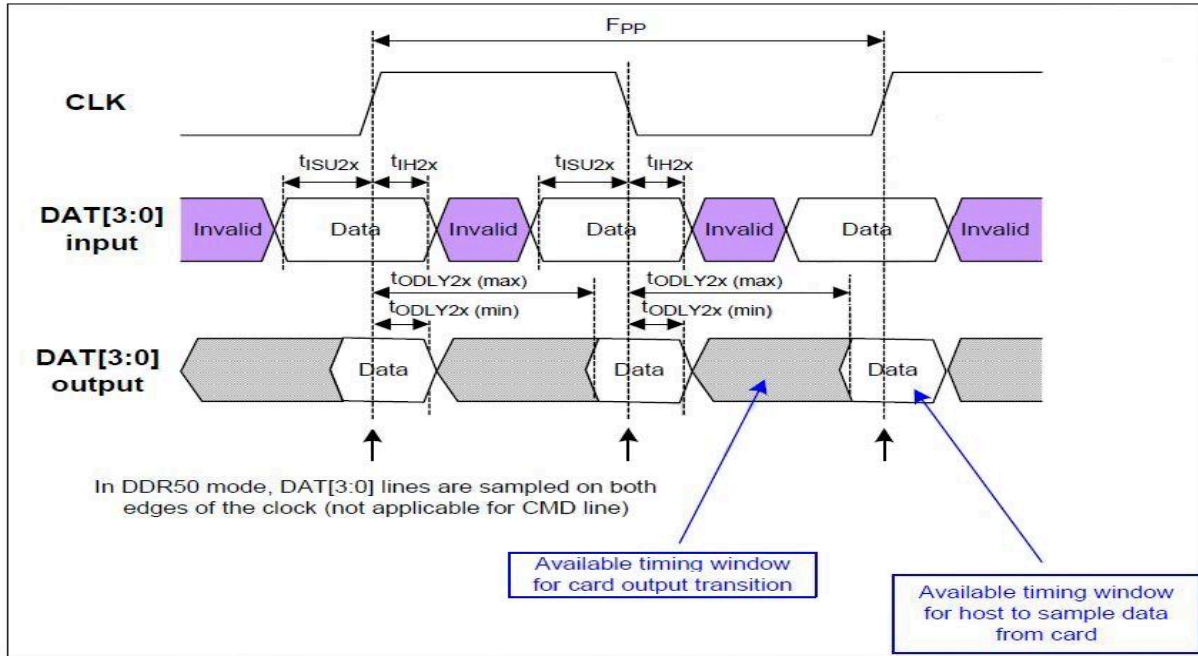
Table 15: Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	t_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

8   REGISTERS

The registers are used in the SMART SD cards are shown in the table below. These registers are described in the sections that follow.

Table 16: Supported SD Registers

Name	Width	Description
CID	128	Card Identification
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register

8.1   Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the information used during the card identification phase. Every individual Flash card will have a unique identification number. The fields for the CID register are presented in the following table.

Table 17: Card Identification Register (CID) Fields

Bits	Width	Name	Field	Value	
				Industrial	
[127:120]	8	Manufacturer ID	MID	27h	
[119:104]	16	OEM/Application ID	OID	5048h	
[103:64]	40	Product Name	PNM	8GB	SD08G
				16GB	SD16G
				32GB	SD32G
				64GB	SD64G
				128GB	SD128
[63:56]	8	Product Revision	PRV	6.0(60h)	
[55:24]	32	Product Serial Number	PSN[1]	--	
[23:20]	4	Reserved	--	--	
[19:8]	12	Manufacturing Date	MDT[1]	--	
[7:1]	7	CRC7 checksum	CRC	--	
[0]	1	Not used, always 1	-	1b	

[1] The value is defined by the default setting.

8.2   Relative Card Address (RCA)

The Relative Card Address (RCA) register is 16 bits wide. It contains the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the identification procedure. The default value of the RCA register is 0x0000.

8.3 Card Specific Data (CSD)

The Card Specific Data (CSD) register is 128 bits wide. It provides information on how to access the card contents. The fields for the CSD register are presented in the following table.

Table 18: Card Specific Data (CSD) Fields

Bits	Width	Name	Field		Value
[127:126]	2	CSD structure	CSD_STRUCTURE		1h
[125:120]	6	Reserved	--		--
[119:112]	8	Data read access time 1	TAAC		0Eh
[111:104]	8	Data read access time 2	NSAC		00h
[103:96]	8	Max. bus clock frequency	TRAN_SPEED[1]		Variable
[95:84]	12	Card command classes	CCC[2]	8GB 16GB 32GB 64GB 128GB	5B5h
[83:80]	4	Max read block data length	READ_BL_LEN[3]		9h
[79]	1	Partial block read allowed	READ_BL_PARTIAL		0h
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN		0h
[77]	1	Read block misalignment	READ_BLK_MISALIGN		0h
[76]	1	DSR implemented	DSR_IMP		0h
[75:70]	6	Reserved	--		--
[69:48]	22	Device size	C_SIZE[4]	8GB	39B6h
				16GB	7753h
				32GB	E7AFh
				64GB	1CF9Fh
				128GB	3A0E7h
[47]	1	Reserved	--		--
[46]	1	Erase single block enable	ERASE_BLK_EN		1h
[45:39]	7	Erase sector size	SECTOR_SIZE		7Fh
[38:32]	7	Write protect group size	WP_GRP_SIZE		0h
[31]	1	Write protect group enable	WP_GRP_ENABLE		0h
[30:29]	2	Reserved	--		--
[28:26]	3	Write speed factor	R2W_FACTOR		2h
[25:22]	4	Max write data block length	WRITE_BL_LEN[3]		9h
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL		0h
[20:16]	5	Reserved	---		--
[15]	1	File format group	FILE_FORMAT_GRP		0h
[14]	1	Copy Flag	COPY		0h
[13]	1	Permanent write protection	PERM_WRITE_PROTECT		0h
[12]	1	Temporary write protection	TMP_WRITE_PROTECT		0h
[11:10]	2	File Format	FILE_FORMAT		0h
[9:8]	2	Reserved	--		--
[7:1]	7	CRC	CRC		Variable
[0]	1	Not used, always '1'	--		1

[1]   The value depends on the Card Type and mode.

[2]   Support command class: 0, 2, 4, 5, 7, 8 and 10.(Including Basic, Block Read/Write, Erase, Lock Card, Application specific and switch. Not supported command class: 1, 3, 6 and 9 (Including Write-Protection, I/O mode).

[3]   This field is fixed to 9h, which indicates READ_BL_LEN / WRITE_BL_LEN = 512 Byte.

[4]   This field depends upon the Flash used with the controller.

8.4 SD Configuration Register (SCR)

The SD Configuration Register (SCR) is 64 bits wide. It is another configuration register. SCR provides information about the SD card's special features that were configured into the given card. The fields for the SCR register are presented in the following table.

Table 19: SD Configuration Register (SCR) Fields

Bits	Width	Name	Field		Value
[63:60]	4	SCR structure	SCR_STRUCTURE		0h
[59:56]	4	SD card spec. version	SD_SPEC		2h
[55]	1	Data status after erase	DATA_STAT_AFTER_ERASE		0h
[54:52]	3	SD security support	SD_SECURITY		0h
[51:48]	4	DAT bus width support	SD_BUS_WIDTHS		5h
[47]	1	Spec. version 3.00 or higher	SD_SPEC3		1h
[46:43]	4	Extended Security Support	EX_SECURITY		0h
[42]	1	Spec. Version 4.00 or Higher	SD_SPEC4	8GB 32GB	0h
				16GB 64GB 128GB	1h
[41:38]	4	Spec. Version 5.00 or Higher	SD_SPECX		2h
[37:36]	9	Reserved	--		--
[35:32]	2	Command Support bits	CMD_SUPPORT	8GB 32GB	3h
				16GB 64GB 128GB	7h
[31:0]	32	Reserved	--		--

8.5 Operation Condition Register (OCR)

The Operation Condition Register (OCR) register is 32 bits wide. The fields for the OCR register are presented in the following table.

Table 20: Operation Condition Register (OCR) Fields

Bits	Width	VDD Voltage Window	Value (Binary)
[0:6]	7	Reserved	--
[7]	1	Reserved for Low Voltage Range	0
[8:14]	7	Reserved	--
[15]	1	2.7-2.8	1
[16]	1	2.8-2.9	1
[17]	1	2.9-3.0	1
[18]	1	3.0-3.1	1
[19]	1	3.1-3.2	1
[20]	1	3.2-3.3	1
[21]	1	3.3-3.4	1
[22]	1	3.4-3.5	1
[23]	1	3.5-3.6	1
[24]	1	Switching to 1.8V Accepted (S18A)	-- [1]
[25:29]	5	Reserved	--
[30]	1	Card Capacity Status (CCS)	--[2]
[31]	1	Card power up status bit	1[3]

[1]   Only UHS-I card supports this bit.

[2]   This bit is valid only when the card power up status bit is set.

[3]   This bit is set to LOW if the card has not finished the power up routine.

8.6 SD Status Register

The SD Status Register (SSR) is 512 bits wide and provides information about the SD card's proprietary and may be used for application-specific usage. The fields for the SSR register are presented in the following table.

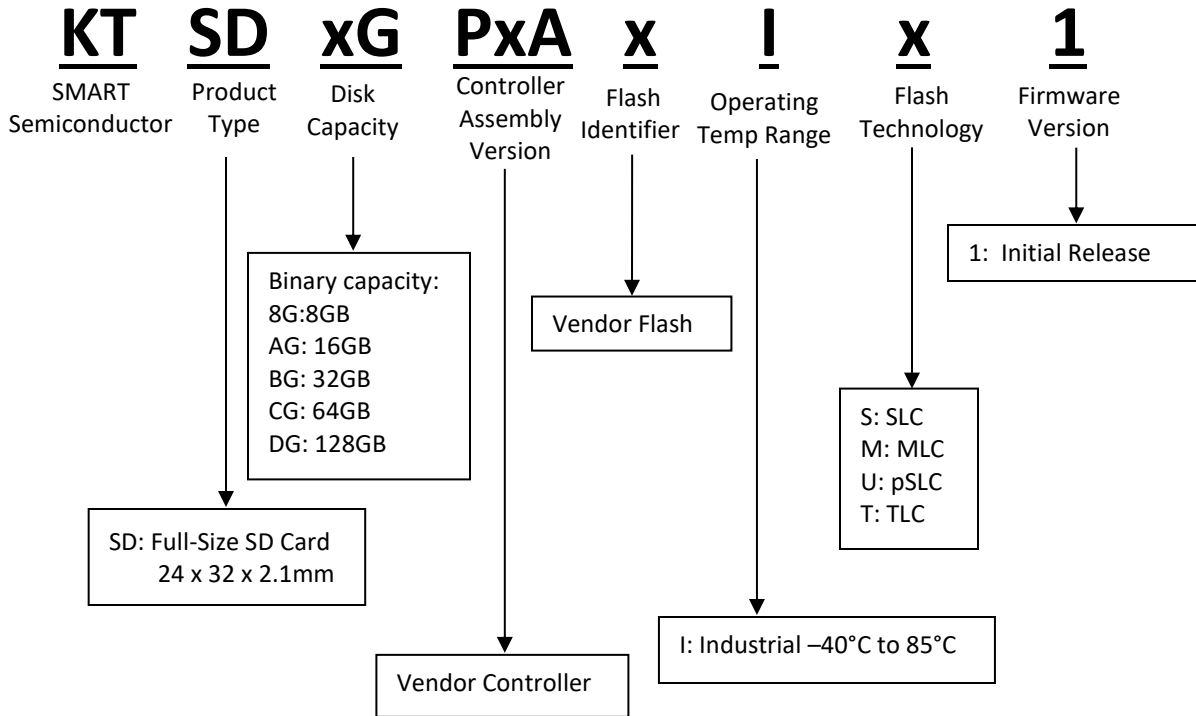**Table 21: SD Status Register (SSR) Fields**

Bits	Width	Field	Value	
[511:510]	2	DAT_BUS_WIDTH	2h	
[509]	1	SECURED_MODE	0h	
[508:502]	7	Reserved for Security Functions	--	
[501:496]	6	Reserved	--	
[495:480]	16	SD_CARD_TYPE	0000h	
[479:448]	32	SIZE_OF_PROTECTED_AREA	8GB	3000000h
			16GB	4000000h
			32GB	5000000h
			64GB	8000000h
			128GB	8000000h
[447:440]	8	SPEED_CLASS	04h	
[439:432]	8	PERFORMANCE_MOVE	8GB/64GB/128GB	0h
			16GB/32GB	3h
[431:428]	4	AU_SIZE	09h	
[427:424]	4	Reserved	--	
[423:408]	16	ERASE_SIZE	8GB	40h
			16GB	100h
			32GB/64GB/128GB	1h
[407:402]	6	ERASE_TIMEOUT	8GB	2Ah
			16GB	Ch
			32GB/128GB	6h
			64GB	3h
[401:400]	2	ERASE_OFFSET	3h	
[399:396]	4	UHS_SPEED_GRADE	8GB/32GB	1h
			16GB/64GB/128GB	3h
[395:392]	4	UHS_AU_SIZE	8GB	Fh
			16GB/32GB/64GB/128GB	9h
[391:384]	8	VIDEO_SPEED_CLASS	8GB/32GB	Ah
			16GB/64GB/128GB	1Eh
[383:378]	6	Reserved	--	
[377:368]	10	VSC_AU_SIZE	8GB	40h
			16GB/32GB/64GB/128GB	8h
[367:346]	22	SUS_ADDR	0h	
[345:340]	6	Reserved	--	
[339:336]	4	APP_PERF_CLASS	8GB	0h
			32GB	1h
			16GB/64GB/128GB	2h
[335:328]	8	PERFORMANCE_ENHANCE	8GB/32GB	0h
			16GB/64GB/128GB	FFh
[327:314]	14	Reserved	--	
[313]	1	DISCARD_SUPPORT	8GB/32GB	0h
			16GB/64GB128GB	1h
[312]	1	FULE_SUPPORT	8GB/32GB	0h
			16GB/64GB128GB	1h
[311:0]	312	Reserved for manufacturer	--	

9 PART NUMBERS

Table 22: Part Numbering Information

Capacity	Part Number
8GB	KTSD8GP3ASIM1
16GB	KTSDAGP2AKIU1
32GB	KTSDBGP1AMIT1
64GB	KTSDCGP2AKIT1
128GB	KTSDDGP2AKIT1

9.1 Part Number Decoder

KT — SMART Semiconductor

SD — Product Type

xG — Disk Capacity

PxA — Controller Assembly Version

x — Flash Identifier

I — Operating Temp Range

x — Flash Technology

1 — Firmware Version

Binary capacity:
8G: 8GB
AG: 16GB
BG: 32GB
CG: 64GB
DG: 128GB

SD: Full-Size SD Card
24 x 32 x 2.1mm

Vendor Controller

Vendor Flash

I: Industrial –40°C to 85°C

S: SLC
M: MLC
U: pSLC
T: TLC

1: Initial Release

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