SMARTsemi
Memory Card Datasheet

Industrial Grade microSD™ Card

September 2023
Rev 3.0

REVISION HISTORY

Date	Revision	Section(s)	Description
June 2023	1.0	All	Initial Release
August 2023	2.0	Performance	Updated Performance data.
September 2023	3.0	Registers	Updated CID table.

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

TABLE OF CONTENTS

1 GENERAL DESCRIPTION 6
1.1 Overview 6
1.2 Features 7
1.3 Unique Features 7
2 OPERATIONAL CHARACTERISTICS 8
2.1 Performance 8
2.2 Power Consumption 8
2.3 Data Retention 8
2.4 Failure Rate 8
2.5 Environmental Conditions 9
2.6 Endurance 9
2.7 Physical Characteristics 9
2.8 Data Reliability 9
3 PRODUCT DESCRIPTION 10
3.1 Functional Block Diagram 10
4 MECHANICAL SPECIFICATIONS 11
4.1 Mechanical Dimensions 11
5 ELECTRICAL SPECIFICATION 12
5.1 Electrical Interface 12
5.2 Absolute Maximum Ratings 13
6 DC CHARACTERISTICS 14
6.1 Bus Operation Conditions for 3.3V Signaling 14
6.2 Bus Operation Conditions for 1.8V Signaling 14
6.3 microSD Memory Card Hardware Interface 15
6.4 Bus Signal Line Loading (Recommended) 15
7 AC CHARACTERISTICS 16
7.1 Interface Timing (Default Speed Mode) 16
7.2 Interface Timing (High Speed Mode) 18
7.3 Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes) 19
7.4 Interface Timing (DDR50 Mode) 21
8 REGISTERS 23
8.1 Card Identification Register (CID) 23
8.2 Relative Card Address (RCA) 23
8.3 Card Specific Data (CSD) 23
8.4 SD Configuration Register (SCR) 25
8.5 Operation Condition Register (OCR) 26
8.6 SD Status Register 27
9 PART NUMBERS 28
9.1 Part Number Decoder 29

LIST OF FIGURES

Figure 1: microSD Block Diagram 10
Figure 2: microSD Dimensions – (in mm) 11
Figure 3: Bus Circuitry Diagram 15
Figure 4: Bus Signal Level 16
Figure 5: Card Input Timing (Default Speed Mode) 16
Figure 6: Card Output Timing (Default Mode) 17
Figure 7: Input Timing (High Speed Mode) 18
Figure 8: Output Timing (High Speed Mode) 18
Figure 9: Input Clock Signal Timing 19
Figure 10: Card Input Timing (SDR50 and SDR104) 20
Figure 11: Output Timing - Fixed Data Window (SDR12, SD25 and SDR50) 20
Figure 12: Output Timing - Variable Window (SDR104) 21
Figure 13: Interface Timing (DDR50 Mode) 21
Figure 14: DAT Inputs/Outputs Referenced to CLK in DDR50 Mode 22

LIST OF TABLES

Table 1: Performance Table 8
Table 2: Current Consumption 8
Table 3: Data Retention 8
Table 4: Failure Rate 8
Table 5: Environmental Conditions and Test Conditions 9
Table 6: Endurance 9
Table 7: Physical Characteristics 9
Table 8: Pinout Assignments and Pin Types 12
Table 9: Absolute Maximum Ratings (1) 13
Table 10: Threshold Level for High Voltage Range 14
Table 11: Peak Voltage and Leakage Current 14
Table 12: Threshold Level for 1.8 V Signaling 14
Table 13: Input Leakage Current for 1.8V Signaling 14
Table 14: Bus Signal Line Loading (Recommended) 15
Table 15: Bus Timing (Default Speed Mode) 17
Table 16: Bus Timing (High Speed) 19
Table 17: Bus Timings – Parameters Values (DDR50 Mode) 22
Table 18: Supported SD Registers 23
Table 19: Card Identification Register (CID) Fields 23
Table 20: Card Specific Data (CSD) Fields 24
Table 21: SD Configuration Register (SCR) Fields 25
Table 22: Operation Condition Register (OCR) Fields 26
Table 23: SD Status Register (SSR) Fields 27
Table 24: Part Numbering Information 28

1 GENERAL DESCRIPTION

1.1 Overview

SMARTsemi's microSD Memory Card product is specifically target at the needs of OEM markets such as networking, telecommunications and data communications. SMARTsemi's microSD products are also a natural fit for mobile and embedded computing, medical, automotive and industrial applications.

SMARTsemi's microSD products offer reliable, high performance operation in an industry standard ultrasonic welded SD housing. They are available in 256 GB capacity.

Incorporating on-board error detection and correction algorithms and static and dynamic wear leveling techniques insure SMARTsemi's microSD products provide years of reliable operation.

SMARTsemi has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMARTsemi engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

1.2 Features

- **Form Factor:** microSD Memory card
- **Capacity:** 256GB
- **NAND Flash:** 3D TLC
- **Performance:**
  - Sequential Read: Up to 97MB/s
  - Sequential Write: Up to 83MB/s
- **Interface:**
  - Compliant with SD specification v6.1
  - Support Application Performance Class 2 (A2)
- **Operating Temperature:**
  - Industrial**:** -40ºC to +85ºC
- **Input Power:** 2.7 V – 3.6 V
- **Dimension**s: 11 mm(L) x 15 mm(W) x 1 mm(H)

1.3 Unique Features

- Global Wear Leveling
- LDPC ECC Engine
- Garbage collection
- Bad block Management
- S.M.A.R.T. Monitor
- RoHS and REACH compliant

2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Table

Capacity	Sequential Read (MB/s)	Sequential Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
256GB	97	83	9400	7200

Note: Sequential performance measured using Crystal Disk. Random performance measured using TestMetrix A2 Test script.

2.2 Power Consumption

Table 2: Current Consumption

Parameter	256GB	Unit (Typical)
Write	215	mA
Read	175	mA
Standby	0.5	mA

Note:

1. The testing result is measured by Crystal Disk Mark 5.1.2
2. The measurement may vary among different host systems and settings.

2.3 Data Retention

Table 3: Data Retention

Item	Value
Data Retention (@ 40˚C)	10 years > 90% life remaining
	1 year < 10% life remaining

2.4 Failure Rate

Table 4: Failure Rate

Item	Value
Mean Time Between Failures (MTBF) (@ 25˚C)	> 3 Million hours

2.5 Environmental Conditions

Table 5: Environmental Conditions and Test Conditions

Parameter	Value
Operating Temperature – Industrial Grade	-40°C to 85°C
Storage Temperature	-55°C to 95°C

2.6 Endurance

Table 6: Endurance

Capacity	Value(Max)
256GB	440 TBW

Note: The result based on JESD219 client workload.

2.7 Physical Characteristics

Table 7: Physical Characteristics

Parameter	Value
Length	11.0 mm
Width	15.0 mm
Height	1.0 mm
Weight (max)	0.25 g

2.8 Data Reliability

- **Global Wear Leveling:** This feature eliminates overstressing Flash media by spreading the data writes across all Flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.

- **LDPC ECC Engine:** To detect and correct errors occur during Read process, ensure data been read correctly. As well as protect data from corruption.

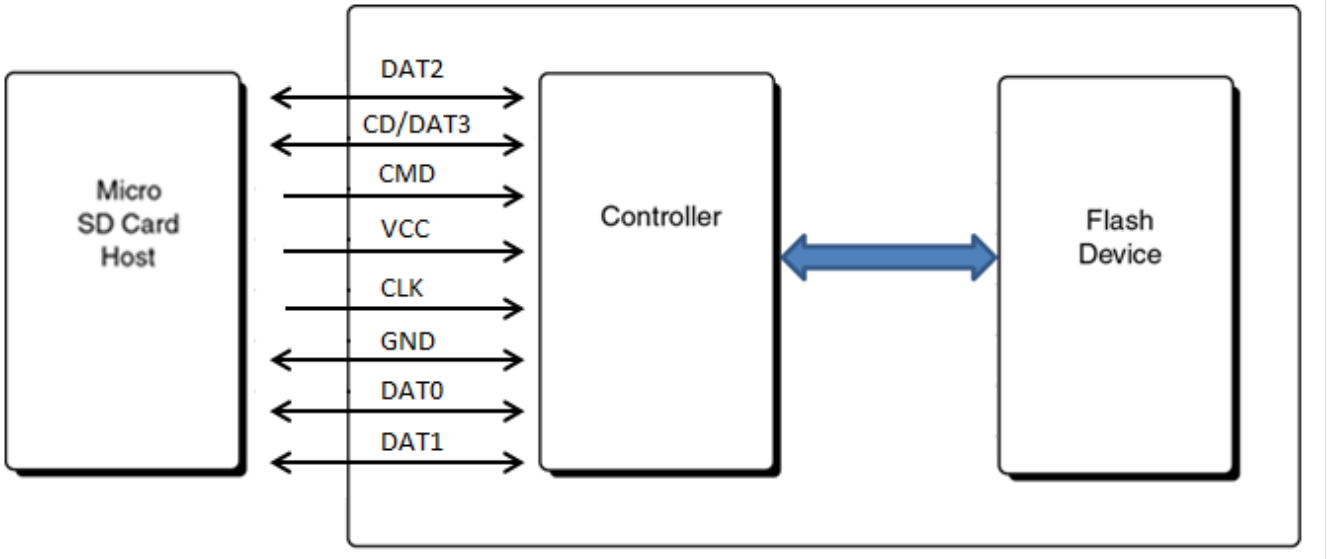
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of Flash media and replaces them with new ones from the spare pool.

3 PRODUCT DESCRIPTION

SMARTsemi's microSD Memory Card product line is offered with an advanced connector. It contains a controller and at least one Flash memory device. The on-board controller interfaces with a microSD Card Host allowing data to be written to and read from the Flash memory device(s).

3.1 Functional Block Diagram

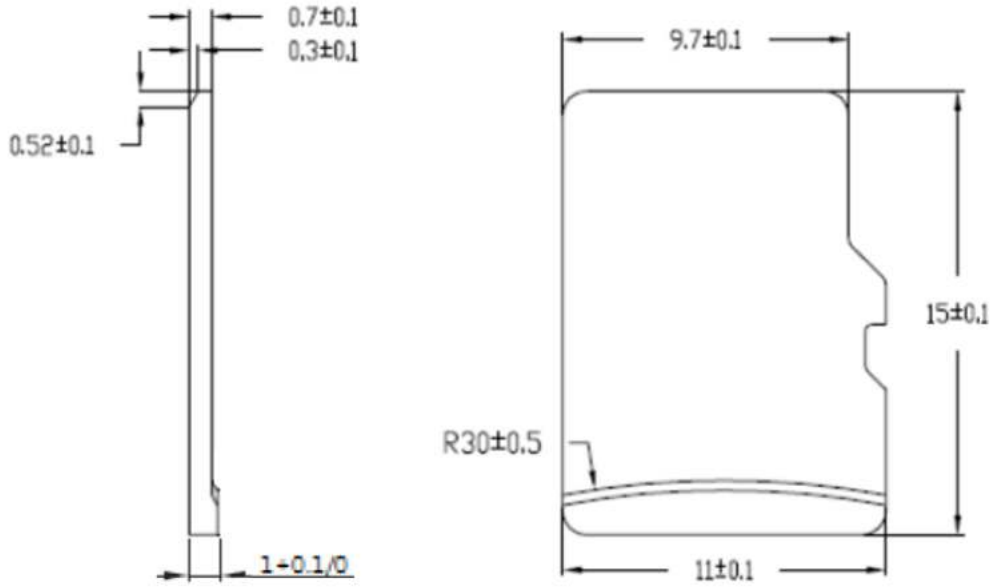
Figure 1: microSD Block Diagram



4 MECHANICAL SPECIFICATIONS

4.1 Mechanical Dimensions

Figure 2: microSD Dimensions – (in mm)



5 ELECTRICAL SPECIFICATION

5.1 Electrical Interface

The SMARTsemi microSD Memory Cards are fully compliant with the SD specification (v6.1). The following table describes the I/O signals of the card. Signals whose source is the Host are designated as inputs (I), while signals that the microSD Card sources are outputs (O). Bi-directional signals are designated as Input/output (I/O).

Figure 3. Pinout Assignments

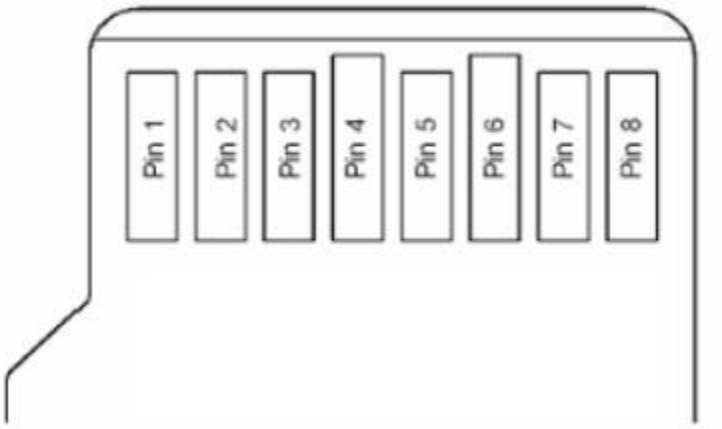


Table 8: Pinout Assignments and Pin Types

Pin	Signal Name	Signal Type[1]	Signal Description
1	DAT2	I/O,PP	SD Interface Bus [2]
2	DAT3[2]	I/O,PP[3]	SD Interface Bus [3]
3	CMD	I/O,PP	Command/Response
4	VDD	S	Power Supply for SD Interface
5	CLK	I	Clock Input
6	VSS2	S	Ground
7	DAT0	I/O,PP	SD Interface Bus [0]
8	DAT1	I/O,PP	SD Interface Bus [1]

1. Type Key: S=power supply; I=input; O=output using push-pull drivers; PP=I/O using push-pull drivers
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode as well while they are not used. It is defined so in order to keep compatibility to MultiMedia Cards.
3. At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

5.2 Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings (1)

Parameter	Minimum Value	Maximum Value	Unit
3.3 V Supply Voltage	-0.3	3.6	V
3.3 V Input Voltage	GND - 0.3	VCC + 0.3	V
Operating Current	-	800	mA
Operating Temperature – (Industrial)	-40	+85	°C
Storage Temperature – (Industrial)	-55	+95	°C

(1) Stress beyond the Absolute Maximum Rating conditions may result in permanent damage to the device. These are stress ratings only and functional operation should be restricted to those indicated in the operational sections of this specification. Exposure to conditions beyond recommended, up to and including the Absolute Maximum Rating conditions, for extended periods may affect device reliability.

6 DC CHARACTERISTICS

6.1 Bus Operation Conditions for 3.3V Signaling

Table 10: Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 11: Peak Voltage and Leakage Current

Parameter	Min.	Max	Unit
Peak voltage on all lines	-0.3	V_{DD}+0.3	V
All Inputs			
Input Leakage Current	-10	10	µA
All Outputs			
Output Leakage Current	-10	10	µA

6.2 Bus Operation Conditions for 1.8V Signaling

Table 12: Threshold Level for 1.8 V Signaling

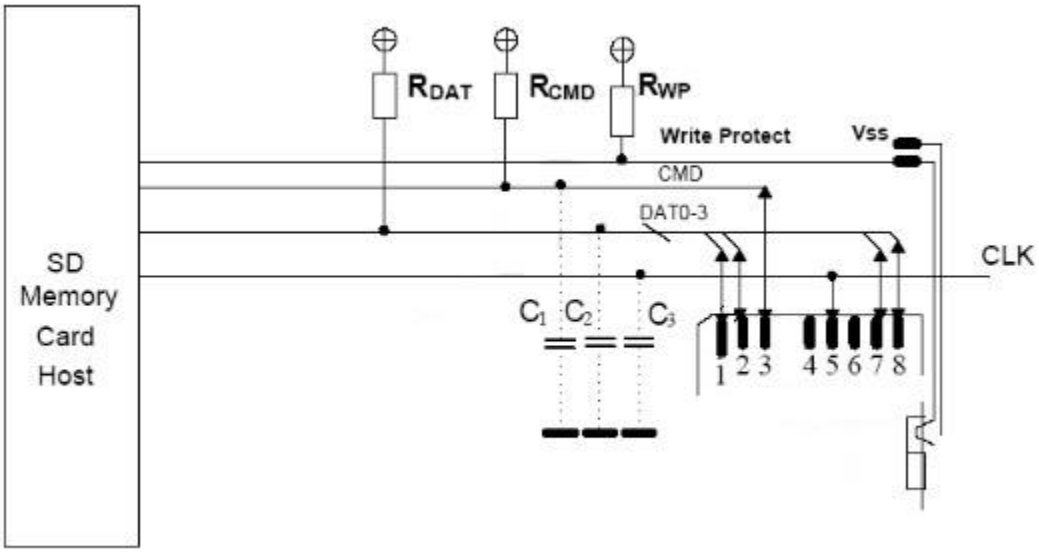
Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Supply Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH}=-2mA
Output Low Voltage	V_{OL}		0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

Table 13: Input Leakage Current for 1.8V Signaling

Parameter	Min.	Max	Unit	Remarks
Input Leakage Current	-2	2	µA	DAT3 pull-up is disconnected.

6.3 microSD Memory Card Hardware Interface

Figure 3: Bus Circuitry Diagram



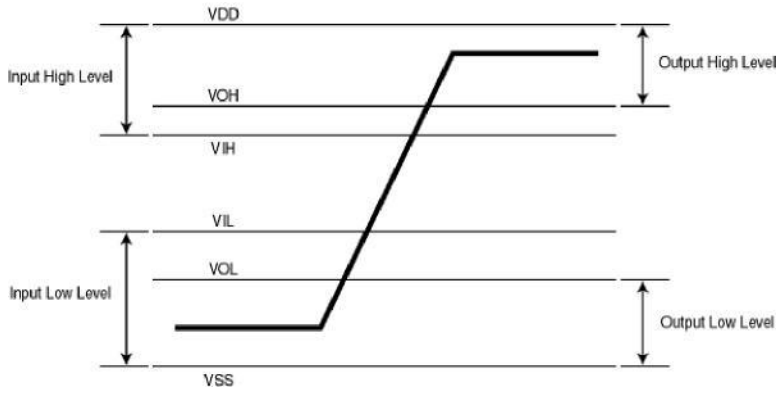
6.4 Bus Signal Line Loading (Recommended)

Table 14: Bus Signal Line Loading (Recommended)

Symbol	Parameter	Min	Max	Units	Remark
R_{CMD}	Pull-up Resistor for CMD Signal	10	100	kΩ	to prevent bus floating
R_{DAT}	Pull-up Resistor for DAT Signals	10	100	kΩ	to prevent bus floating
C_L	Total bus capacitance for each signal line		40	pF	1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF
C_{CARD}	Card Capacitance for each signal pin		10	pF	
-	Maximum signal line inductance		16	nH	
R_{DAT3}	Pull-up resistance inside card	10	90	kΩ	May be used for card detection
C_C	Capacity Connected to Power Line		5	μF	To prevent inrush current

7 AC CHARACTERISTICS

Figure 4: Bus Signal Level



7.1 Interface Timing (Default Speed Mode)

Figure 5: Card Input Timing (Default Speed Mode)

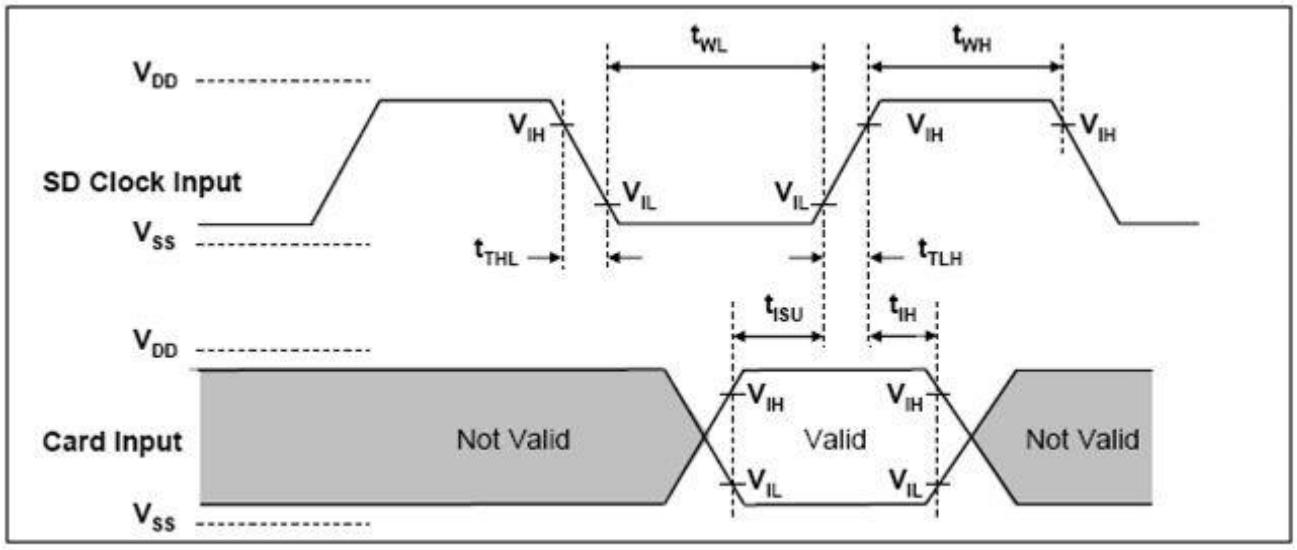


Figure 6: Card Output Timing (Default Mode)

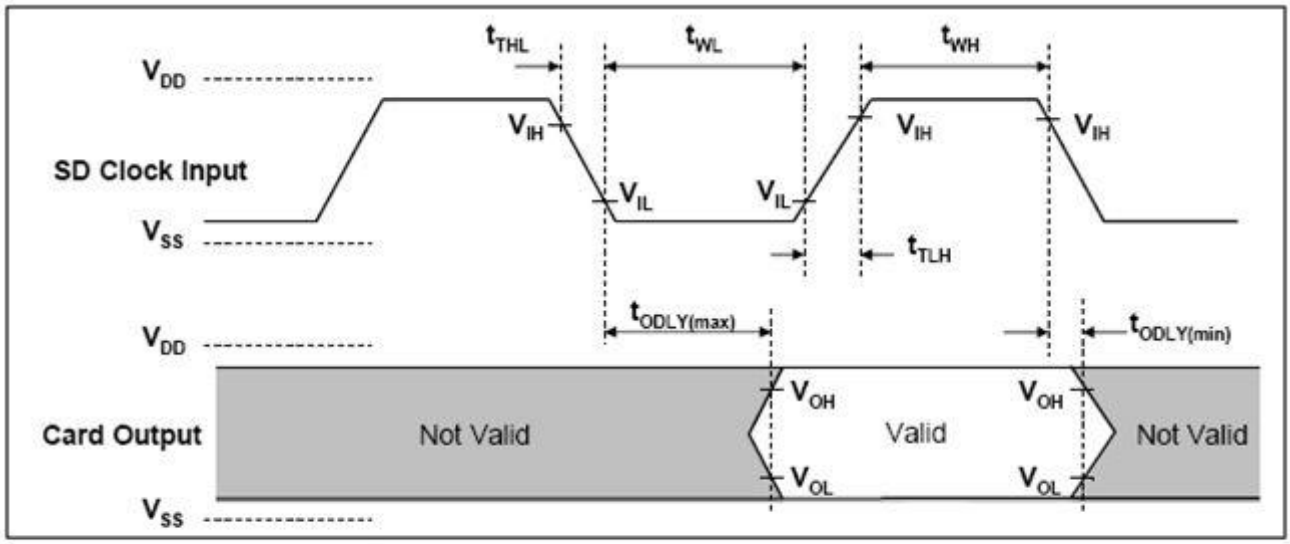


Table 15: Bus Timing (Default Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark (1)
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency data transfer mode	0	25	MHz	C_{card} ≤ 10 pF
f_{OD}	Clock frequency Identification Mode	0(2)/100	400	kHz	
t_{WL}	Clock low time	10		ns	C_{card} ≤ 10 pF
t_{WH}	Clock high time	10		ns	C_{card} ≤ 10 pF
t_{TLH}	Clock rise time		10	ns	C_{card} ≤ 10 pF
t_{THL}	Clock fall time		10	ns	C_{card} ≤ 10 pF
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	5		ns	C_{card} ≤ 10 pF
t_{IH}	Input hold time	5		ns	C_{card} ≤ 10 pF
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output delay time during Data Transfer Mode	0	14	ns	C_L ≤ 40 pF
t_{ODLY}	Output delay time during Data Identification mode	0	50	ns	C_L ≤ 40 pF

1. Values are for 1 card.
2. 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

7.2 Interface Timing (High Speed Mode)

Figure 7: Input Timing (High Speed Mode)

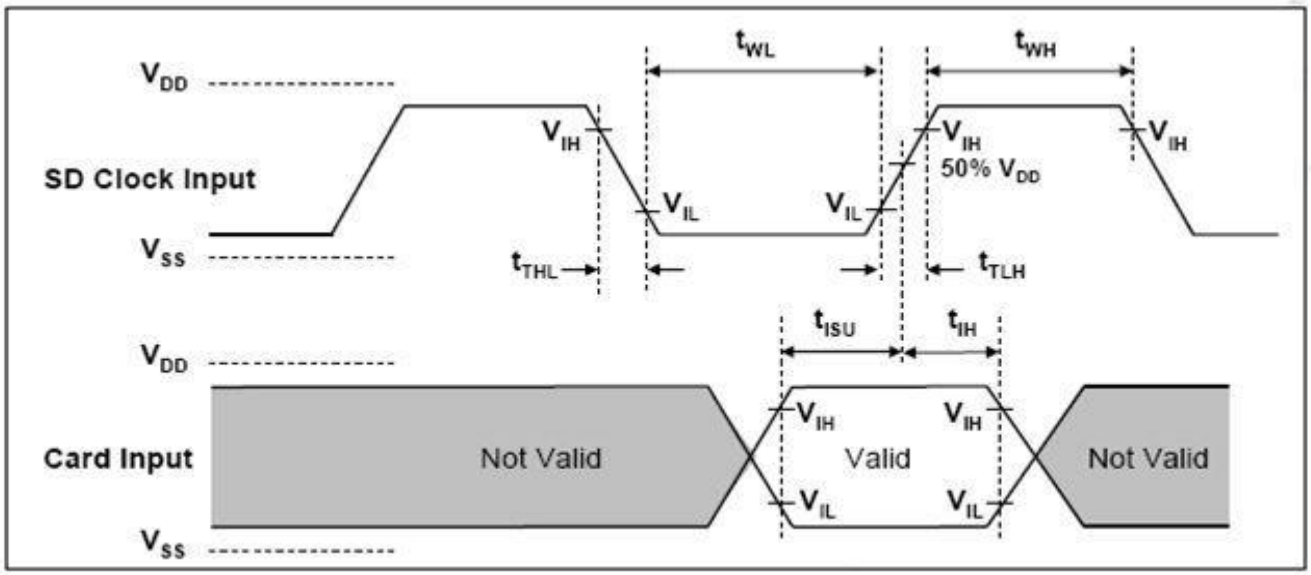


Figure 8: Output Timing (High Speed Mode)

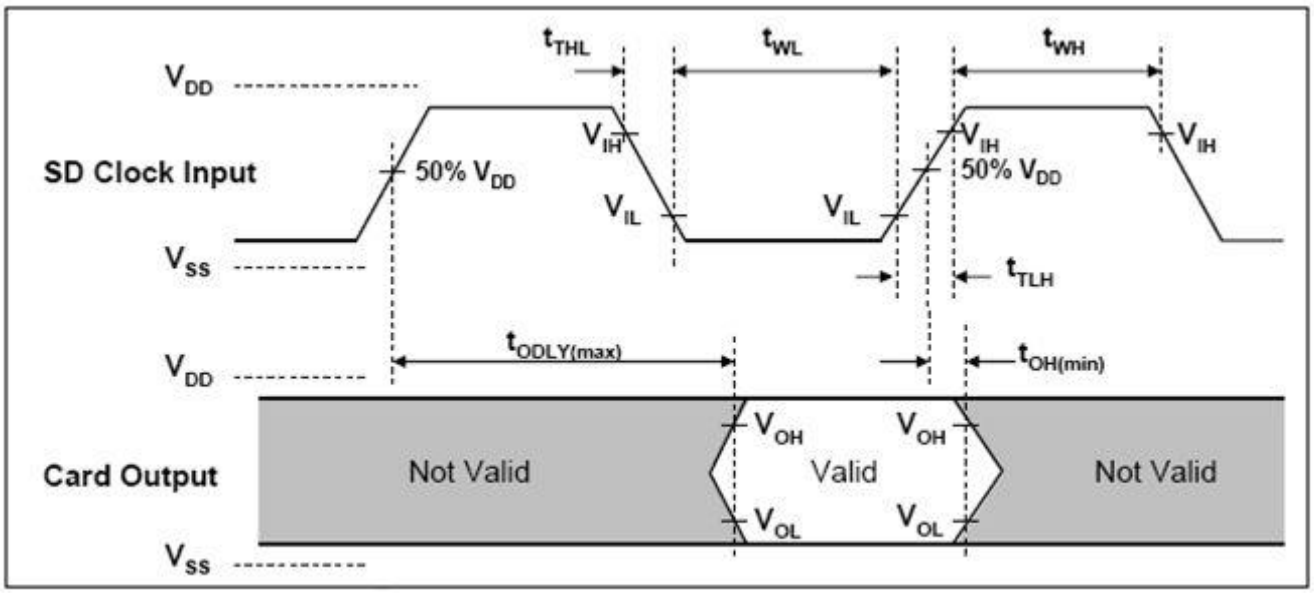


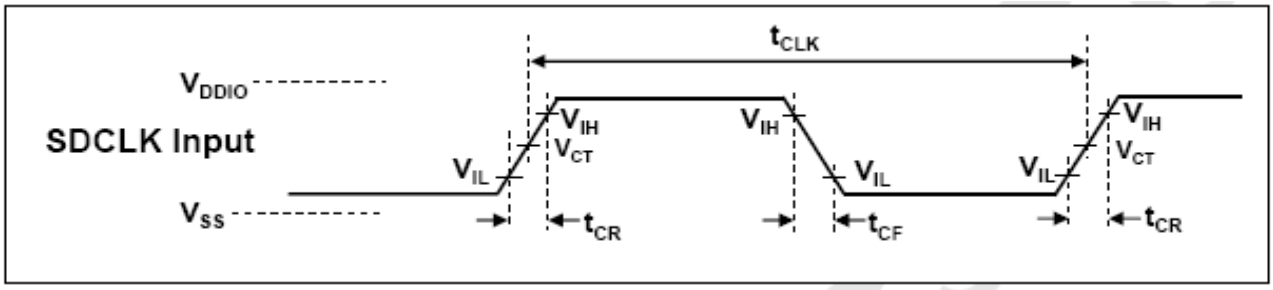
Table 16: Bus Timing (High Speed)

Symbol	Parameter	Min	Max	Unit	Remark[1]
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f_{PP}	Clock frequency data transfer mode	0	50	MHz	C_{card} ≤ 10 pF
t_{WL}	Clock low time	7	-	ns	C_{card} ≤ 10 pF
t_{WH}	Clock high time	7	-	ns	C_{card} ≤ 10 pF
t_{TLH}	Clock rise time	-	3	ns	C_{card} ≤ 10 pF
t_{THL}	Clock fall time	-	3	ns	C_{card} ≤ 10 pF
Inputs CMD, DAT (referenced to CLK)					
t_{ISU}	Input setup time	6	-	ns	C_{card} ≤ 10 pF
t_{IH}	Input hold time	2	-	ns	C_{card} ≤ 10 pF
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output delay time during Data Transfer Mode	-	14	ns	C_L ≤ 40 pF
t_{OH}	Output Hold Time	2.5	-	ns	C_L ≤ 15 pF
c_L	Total System Capacitance of each line	-	40	pF	C_L ≤ 15 pF

1. In order to satisfy server timing, host shall drive only one card.

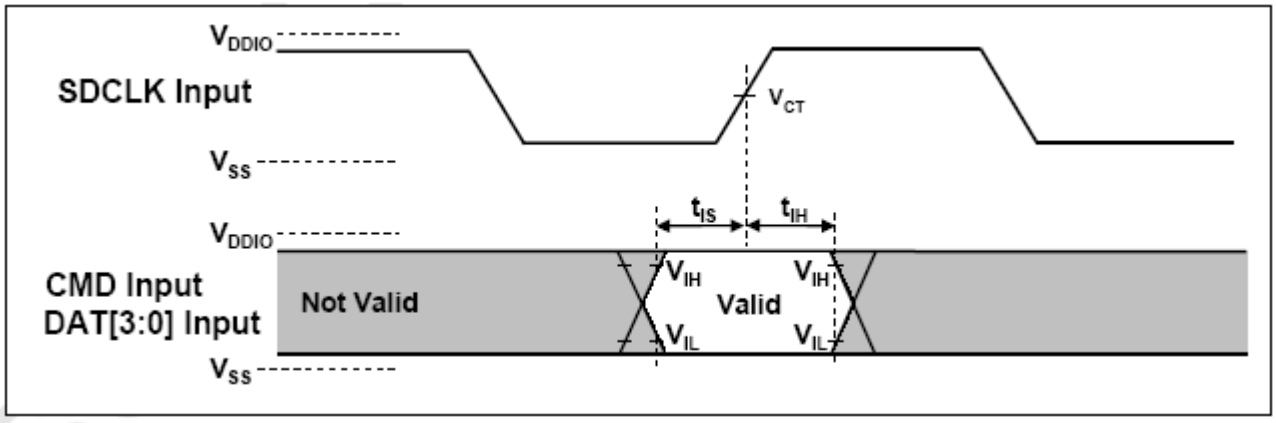
7.3 Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes)

Figure 9: Input Clock Signal Timing



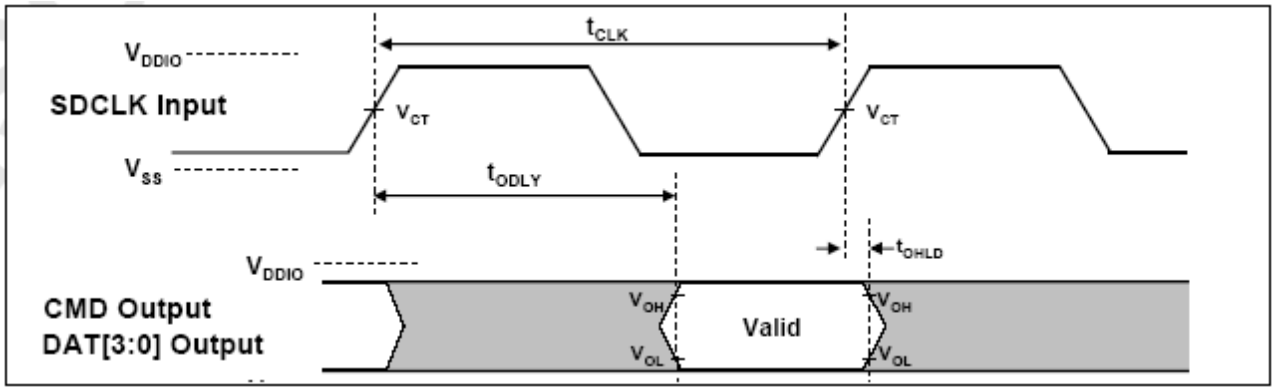
Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD} =10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD} =10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

Figure 10: Card Input Timing (SDR50 and SDR104)



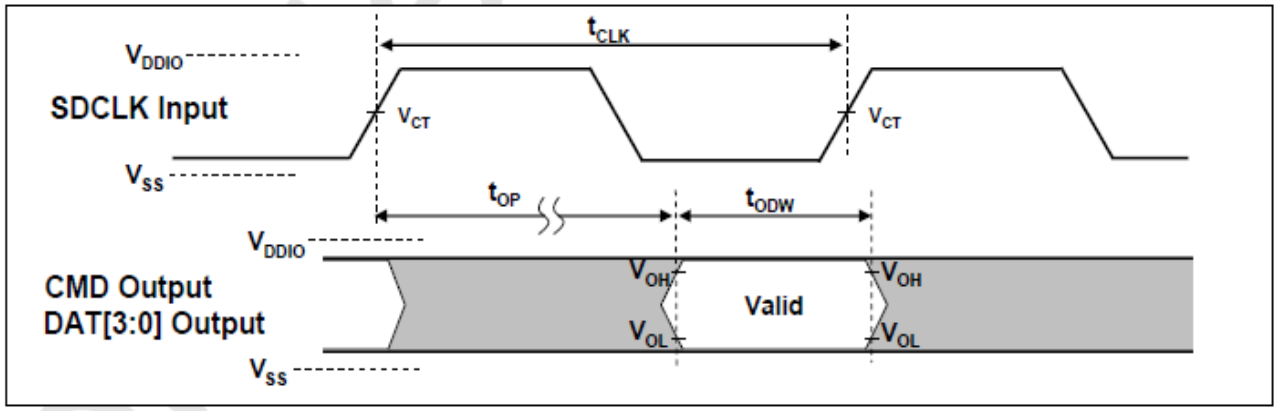
Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

Figure 11: Output Timing - Fixed Data Window (SDR12, SD25 and SDR50)



Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, CL=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, CL=40pF, using driver Type B, for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

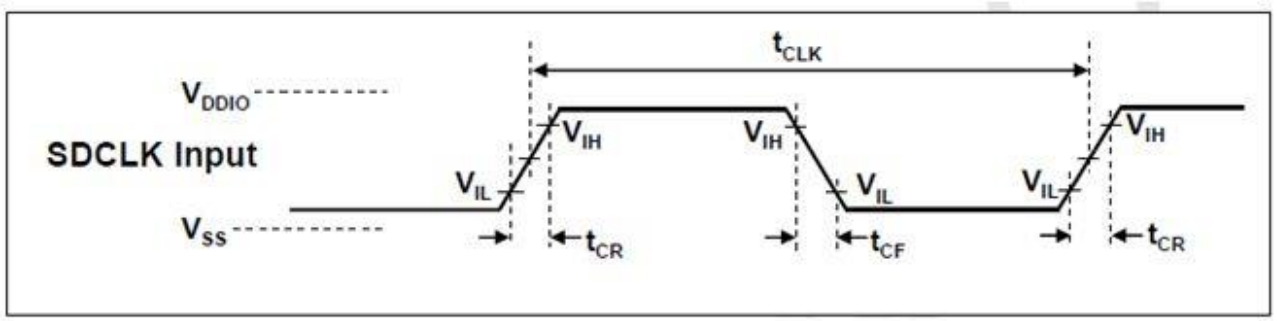
Figure 12: Output Timing - Variable Window (SDR104)



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δ_{tOP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

7.4 Interface Timing (DDR50 Mode)

Figure 13: Interface Timing (DDR50 Mode)



Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max) Between rising edge
t_{CR}, t_{CF}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (Max) at 50MHz, C_{CARD} = 10pF
Clock Duty	45	55	%	

Figure 14: DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

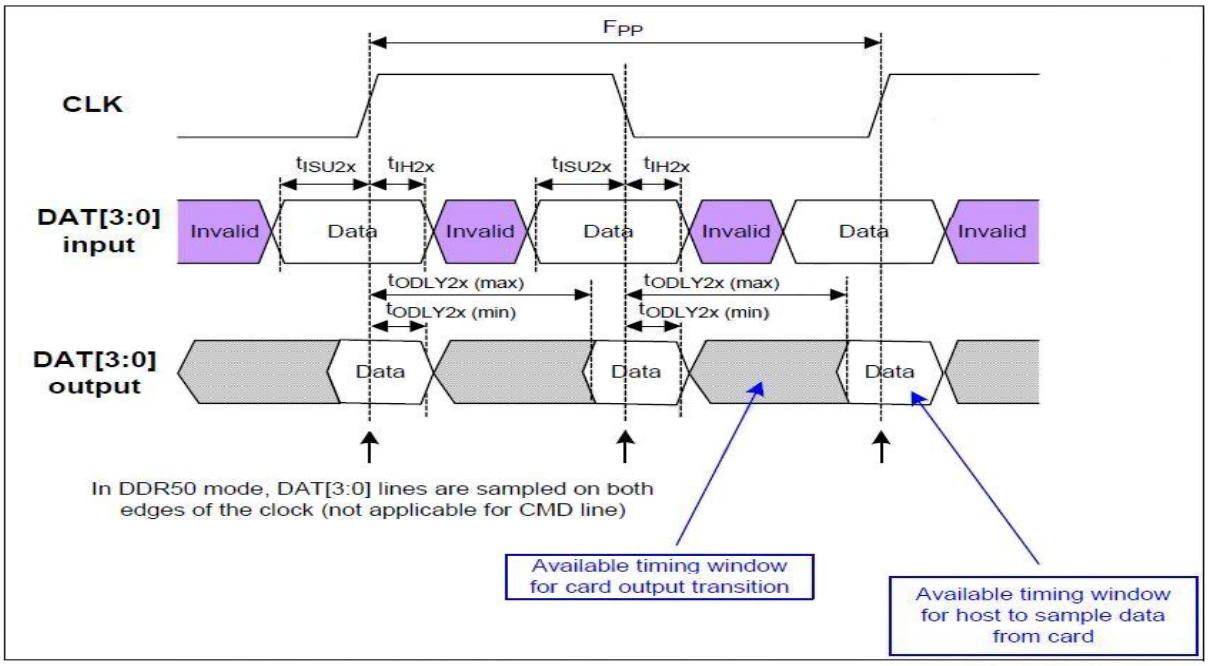


Table 17: Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L≤30 pF (1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_L≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{card}≤ 10 pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{card}≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25 pF (1 card)
Output Hold time	t_{OH2x}	1.5	-	ns	C_L≥15 pF (1 card)

8 REGISTERS

The registers are used in the SMART microSD cards are shown in the table below. These registers are described in the sections that follow.

Table 18: Supported SD Registers

Name	Width	Description
CID	128	Card Identification
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register

8.1 Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the information used during the card identification phase. Every individual Flash card will have a unique identification number. The fields for the CID register are presented in the following table.

Table 19: Card Identification Register (CID) Fields

Bits	Width	Name	Field	Value
				Industrial
[127:120]	8	Manufacturer ID	MID	1Dh
[119:104]	16	OEM/Application ID	OID	4144h
[103:64]	40	Product Name	PNM	SD256
[63:56]	8	Product Revision	PRV	10h
[55:24]	32	Product Serial Number	PSN(1)	--
[23:20]	4	Reserved	--	--
[19:8]	12	Manufacturing Date	MDT(1)	--
[7:1]	7	CRC7 checksum	CRC	--
[0]	1	Not used, always 1	-	1b

(1) The value is defined by the default setting.

8.2 Relative Card Address (RCA)

The Relative Card Address (RCA) register is 16 bits wide. It contains the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the identification procedure. The default value of the RCA register is 0x0000.

8.3 Card Specific Data (CSD)

The Card Specific Data (CSD) register is 128 bits wide. It provides information on how to access the card contents. The fields for the CSD register are presented in the following table.

Table 20: Card Specific Data (CSD) Fields

Bits	Width	Name	Field	Value
[127:126]	2	CSD structure	CSD_STRUCTURE	1h
[125:120]	6	Reserved	--	--
[119:112]	8	Data read access time 1	TAAC	0Eh
[111:104]	8	Data read access time 2	NSAC	00h
[103:96]	8	Max. bus clock frequency	TRAN_SPEED(1)	32h
[95:84]	12	Card command classes	CCC(2)	DB7h
[83:80]	4	Max read block data length	READ_BL_LEN(3)	9h
[79]	1	Partial block read allowed	READ_BL_PARTIAL	0h
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	0h
[77]	1	Read block misalignment	READ_BLK_MISALIGN	0h
[76]	1	DSR implemented	DSR_IMP	0h
[75:70]	6	Reserved	--	--
[69:48]	22	Device size	C_SIZE(4)	75C7Dh
[47]	1	Reserved	--	--
[46]	1	Erase single block enable	ERASE_BLK_EN	1h
[45:39]	7	Erase sector size	SECTOR_SIZE	7Fh
[38:32]	7	Write protect group size	WP_GRP_SIZE	0h
[31]	1	Write protect group enable	WP_GRP_ENABLE	0h
[30:29]	2	Reserved	--	--
[28:26]	3	Write speed factor	R2W_FACTOR	2h
[25:22]	4	Max write data block length	WRITE_BL_LEN(3)	9h
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	0h
[20:16]	5	Reserved	---	--
[15]	1	File format group	FILE_FORMAT_GRP	0h
[14]	1	Copy Flag	COPY	0h
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0h
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0h
[11:10]	2	File Format	FILE_FORMAT	0h
[9:8]	2	Reserved	--	--
[7:1]	7	CRC	CRC	33h
[0]	1	Not used, always ‘1’	--	1

(1) The default value is 32h. The value depends on the Card Type and mode.

(2) Support command class: 0, 2, 4, 5, 7, 8 and 10.(Including Basic, Block Read/Write, Erase, Lock Card, Application specific and switch. Not supported command class: 1, 3, 6 and 9 (Including Write-Protection, I/O mode).

(3) This field is fixed to 9h, which indicates READ_BL_LEN / WRITE_BL_LEN = 512 Byte.

(4) This field depends upon the Flash used with the controller.

8.4 SD Configuration Register (SCR)

The SD Configuration Register (SCR) is 64 bits wide. It is another configuration register. SCR provides information about the microSD card's special features that were configured into the given card. The fields for the SCR register are presented in the following table.

Table 21: SD Configuration Register (SCR) Fields

Bits	Width	Name	Field	Value
[63:60]	4	SCR structure	SCR_STRUCTURE	0h
[59:56]	4	SD card spec. version	SD_SPEC	2h
[55]	1	Data status after erase	DATA_STAT_AFTER_ERASE	0h
[54:52]	3	SD security support	SD_SECURITY	0h
[51:48]	4	DAT bus width support	SD_BUS_WIDTHS	5h
[47]	1	Spec. version 3.00 or higher	SD_SPEC3	1h
[46:43]	4	Extended Security Support	EX_SECURITY	0h
[42]	1	Spec. Version 4.00 or Higher	SD_SPEC4	1h
[41:38]	4	Spec. Version 5.00 or Higher	SD_SPECX	2h
[37:36]	9	Reserved	--	--
[35:32]	2	Command Support bits	CMD_SUPPORT	7h
[31:0]	32	Reserved	--	--

8.5 Operation Condition Register (OCR)

The Operation Condition Register (OCR) register is 32 bits wide. The fields for the OCR register are presented in the following table.

Table 22: Operation Condition Register (OCR) Fields

Bits	Width	VDD Voltage Window	Value (Binary)
[0:6]	7	Reserved	--
[7]	1	Reserved for Low Voltage Range	0
[8:14]	7	Reserved	--
[15]	1	2.7-2.8	1
[16]	1	2.8-2.9	1
[17]	1	2.9-3.0	1
[18]	1	3.0-3.1	1
[19]	1	3.1-3.2	1
[20]	1	3.2-3.3	1
[21]	1	3.3-3.4	1
[22]	1	3.4-3.5	1
[23]	1	3.5-3.6	1
[24]	1	Switching to 1.8V Accepted (S18A)	-- (1)
[25:29]	5	Reserved	--
[30]	1	Card Capacity Status (CCS)	--(2)
[31]	1	Card power up status bit	1(3)

(1) Only UHS-I card supports this bit.

(2) This bit is valid only when the card power up status bit is set.

(3) This bit is set to LOW if the card has not finished the power up routine.

8.6 SD Status Register

The SD Status Register (SSR) is 512 bits wide and provides information about the SD card's proprietary and may be used for application-specific usage. The fields for the SSR register are presented in the following table.

Table 23: SD Status Register (SSR) Fields

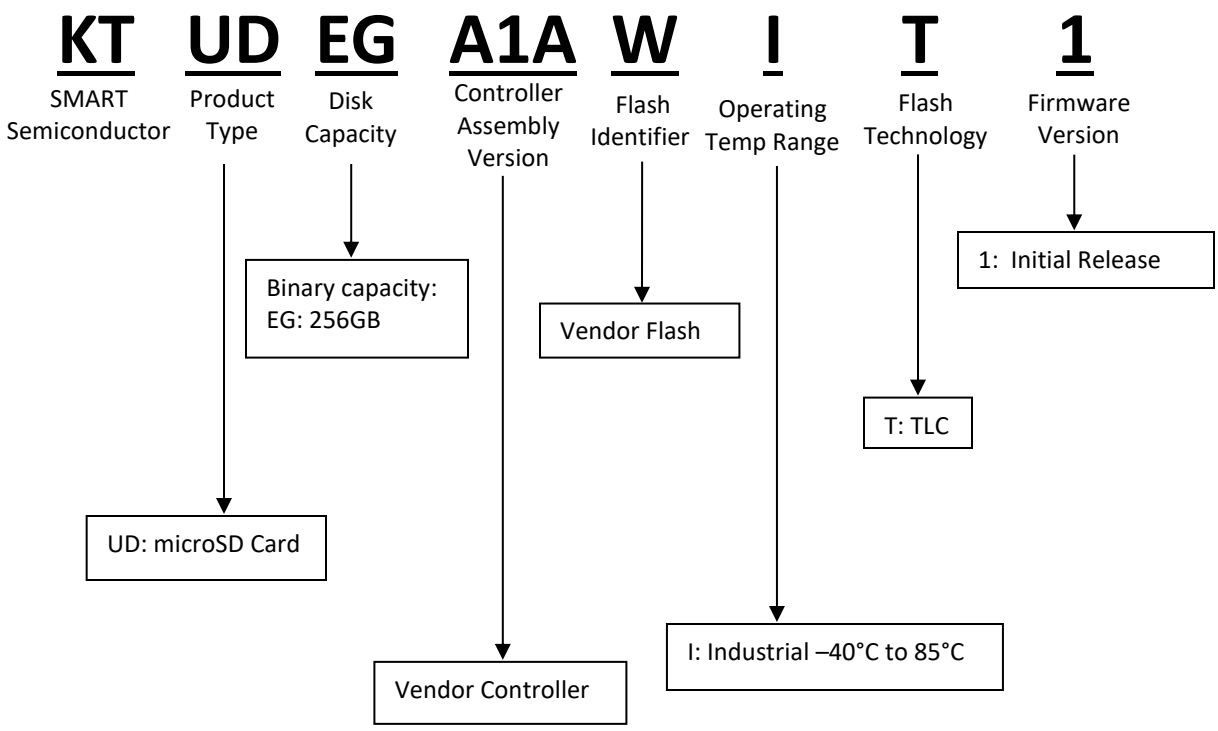
Bits	Width	Field	Value
[511:510]	2	DAT_BUS_WIDTH	2h
[509]	1	SECURED_MODE	0h
[508:502]	7	Reserved for Security Functions	--
[501:496]	6	Reserved	--
[495:480]	16	SD_CARD_TYPE	0000h
[479:448]	32	SIZE_OF_PROTECTED_AREA	8000000h
[447:440]	8	SPEED_CLASS	04h
[439:432]	8	PERFORMANCE_MOVE	0h
[431:428]	4	AU_SIZE	09h
[427:424]	4	Reserved	--
[423:408]	16	ERASE_SIZE	8h
[407:402]	6	ERASE_TIMEOUT	4h
[401:400]	2	ERASE_OFFSET	1h
[399:396]	4	UHS_SPEED_GRADE	3h
[395:392]	4	UHS_AU_SIZE	9h
[391:384]	8	VIDEO_SPEED_CLASS	1Eh
[383:378]	6	Reserved	--
[377:368]	10	VSC_AU_SIZE	8h
[367:346]	22	SUS_ADDR	0h
[345:340]	6	Reserved	--
[339:336]	4	APP_PERF_CLASS	2h
[335:328]	8	PERFORMANCE_ENHANCE	0h
[327:314]	14	Reserved	--
[313]	1	DISCARD_SUPPORT	0h
[312]	1	FULE_SUPPORT	0h
[311:0]	312	Reserved for manufacturer	--

9 PART NUMBERS

Table 24: Part Numbering Information

Capacity	Part Number
256GB	KTUDEGA1AWIT1

9.1 Part Number Decoder



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