Reliability Summary Report

Product Type:	512Mb (32Mx16) DDR2
Part Number:	KTDM522D680BGCEA KTDM522D680BGIEA
Package:	84 ball BGA

1. Features

- JEDEC Standard
- V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V
- Internal pipelined Double-Data-Rate architecture; two data access per clock cycle
- Bi-directional differential data strobe (DQS, $\overline{DQS}$); $\overline{DQS}$ can be disabled for single-ended data strobe operation
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- 8 bank operation
- CAS Latency: 3, 4, 5, 6, 7
- Additive Latency: 0, 1, 2, 3, 4, 5, 6
- Burst Type: Sequential and Interleave
- Burst Length: 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Off-Chip-Driver (OCD) impedance adjustment
- On-Die-Termination for better signal quality
- Special function support
  - 50 / 75 / 150 ohm ODT
  - High Temperature Self refresh rate enable
  - Duty Cycle Corrector
  - Partial Array Self Refresh (PASR)

- Auto & Self refresh
- Refresh cycle:
  - 8192 cycles/64 ms (7.8 µs refresh interval) at 0°C ≤ T_C ≤ +85°C (Commercial) or -40°C ≤ T_C ≤ +85°C (Industrial)
  - 8192 cycles/32 ms (3.9 µs refresh interval) at +85°C < T_C ≤ +95°C
- SSTL_18 interface

2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM522D680BGCEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Commercial	Pb-free
KTDM522D680BGIEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Industrial	Pb-free

Note:

1. The above description is extracted from the datasheet. Please refer to the document for detailed information.

3. Product Qualification – Die Related Tests

3.1. Test Conditions & Results - Life Test

Accelerated Life Stress Test									
Item		High Temperature Operating Life Test		Low Temperature Operating Life Test		High Temperature Bake Test		ELFR	
Condition		Ta = 125°C V ≥ 1.1 x Vcc Dynamic		Ta = -40°C V ≥ 1.1 x Vcc Dynamic		Ta = 150°C		Ta = 125°C V ≥ 1.1 x Vcc Dynamic	
Sample Size		105		105		77		1200	
Test Method		JESD22-A108		JESD22-A108		JESD22-A103		AEC Q100-008	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot2	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot3	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass

3.2. Test Conditions & Results - Environmental Test (84 Ball BGA)

Accelerated Environment Stress Test									
Item		Preconditioning		Pressure Cooker Test (Autoclave)		Highly Accelerated Temperature and Humidity Stress Test		Temperature Cycle Test	
Condition		T/C x 5cyc Bake x 24hrs Moisture soaking (JEDEC level III) IR (260°C) Reflow x3		Ta = 121°C RH = 100% 29.7 Psia, 960 hrs		Ta = 130°C RH = 85% Vstress = 1.98V 33.3 Psia, 100 hrs		55°C (10min) ~ 125°C (10min), Air to Air	
Sample Size		201		55		32		55	
Test Method		JEDEC J-STD-020 JESD22-A113		JESD22-A102		EIA/JESD22-A110 EIA/JESD22-A118		JESD22-A104 MIL-STD883 Method 1010.7	
Accept Criteria		LTPD = 7%		168hrs, LTPD = 7%		100hrs, LTPD = 7%		500 cycles, LTPD = 7%	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/201	Pass	0f/55	Pass	0f/32	Pass	0f/55	Pass
	Lot2	0f/201	Pass	0f/55	Pass	0f/32	Pass	0f/55	Pass
	Lot3	0f/201	Pass	0f/55	Pass	0f/32	Pass	0f/55	Pass

3.3. Test Conditions & Results - Electrical Test

Electrical Verification Test										
Item	ESD						Latch-Up			
Condition	H.B.M		M.M		CDM		Vtrig		Itrig	
Sample Size	5/case		5/case		5/case		5/case		5/case	
Test Method	EIA/JEDEC JESD22-A114		EIA/JESD22-A115		JESD22-C101E		EIA/JESD78			
Accept Criteria	≥2KV		≥200V		±1KV		$>V_{CC}+1.8V$, $<V_{SS}-1.8V$		>± 200mA	
Test Results	Result	Comment	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	>2KV	Pass	>200V	Pass	±1KV	Pass	$>V_{CC}+1.8V$, $<V_{SS}-1.8V$	Pass	>±200 mA	Pass

4. Estimation of Long-term Failure Rate

4.1. Model

L = Aexp(EA/kT)*exp(-BVcc)
Where:
L: Life time
Ea: Activation energy
B: Voltage acceleration factor
T: Absolute temperature
Vcc: Applied voltage

4.2. Statistical Analysis

$\lambda \text{max} = \frac{\chi^2(1-\alpha)}{2t}$ [with df=2(r+1)]

MTBFmin = $^{1}/_{\lambda \text{max}}$

Where:

λmax = Maximum or worst-case failure rate

MTBFmin = Minimum (worst-case) expected MTBF

χ^2 = Chi square distribution

r = Number of failures

df = Degrees of freedon

t = total number of test hours (number of devices x number of hours)

α = Statistical error expected in estimate. For 60% confidence, α = 0.4 or 1-α = 0.6

4.3. Calculation of HTOL Data

Acceleration Factor: Ea = 0.5eV, B = 7.0 (1/V)
Field Condition: Ta = 55°C, Vcc =1.8V
HTOL (Condition)
Acceleration: A_T (125°C:55°C) = 22.45 times
Vcc (2.2V:1.8V) ←→ Vinternal (3.52V:2.9V)
Av (3.52V:2.9V) = 76.71 times

Estimated failure rate = $\frac{1.83 \text{ x } 10^9}{2 \text{ x } (315 \text{ x } 1000) \text{ x } 22.45 \text{ x } 76.71}$

= 1 .69 FIT

Reliability Summary Report

Product Type: 512Mb (32Mx16) DDR2

Part Number: KTDM522D680BGAEA

Package: 84 ball BGA

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1. Features

- JEDEC Standard
- V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V
- Internal pipelined Double-Data-Rate architecture; two data access per clock cycle
- Bi-directional differential data strobe (DQS, $\overline{DQS}$); $\overline{DQS}$ can be disabled for single-ended data strobe operation
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- 8 bank operation
- CAS Latency: 3, 4, 5, 6, 7
- Additive Latency: 0, 1, 2, 3, 4, 5, 6
- Burst Type: Sequential and Interleave
- Burst Length: 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Off-Chip-Driver (OCD) impedance adjustment
- On-Die-Termination for better signal quality
- Special function support
  - 50 / 75 / 150 ohm ODT
  - High Temperature Self refresh rate enable
  - Duty Cycle Corrector
  - Partial Array Self Refresh (PASR)

- Auto & Self refresh
- Refresh cycle:
  - 8192 cycles/64 ms (7.8 µs refresh interval) at -40°C ≤ T_C ≤ +85°C
  - 8192 cycles/32 ms (3.9 µs refresh interval) at +85°C < T_C ≤ +95°C
  - 8192 cycles/16 ms (1.95 µs refresh interval) at +95°C < TC ≤ +105°C
- SSTL_18 interface

2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM522D680BGAEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Automotive	Pb-free

Note:

1. The above description is extracted from the datasheet. Please refer to the document for detailed information.

3. Product Qualification – Die Related Tests

3.1. Test Conditions & Results - Life Test - High Temperature

Accelerated Life Stress Test							
Item		High Temperature Operating Life Test		High Temperature Bake Test		ELFR	
AEC-Q100 Item Test		B1		A2		B2	
Condition		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = 150°C, 1000 hrs		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 72 hrs	
Sample Size		105		77		1200	
Test Method		JESD22-A108		JESD22-A103		AEC Q100-008	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot2	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot3	0f/105	Pass	0f/77	Pass	0f/1200	Pass

3.2. Test Conditions & Results - Life Test - Low Temperature

Accelerated Life Stress Test					
Item		Low Temperature Operating Life Test		Low Temperature Bake Test	
Condition		Ta = -40°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = -40°C, 192 hrs	
Sample Size		105		10	
Test Results	Lot	Result	Comment	Result	Comment
	Lot1	0f/105	Pass	0f/10	Pass
	Lot2	0f/105	Pass	0f/10	Pass
	Lot3	0f/105	Pass	0f/10	Pass

3.3. Test Conditions & Results - Environmental Test (84 Ball BGA)

Accelerated Environment Stress Test									
Item		Preconditioning		Pressure Cooker Test (Autoclave)		Highly Accelerated Temperature and Humidity Stress Test		Temperature Cycle Test	
AEC-Q100 Item Test Number		A1		A2		A2		A4	
Condition		T/C x 5cyc Bake x 24hrs Moisture soaking (JEDEC level III) IR (260°C) Reflow x3		Ta = 121°C RH = 100% 29.7 Psia, 960 hrs		Ta = 130°C RH = 85% Vstress = 1.1 x Vcc 33.3 Psia, 100 hrs		65°C (10min) ~ 150°C (10min), Air to Air, 500 cycles	
Sample Size		238		77		77		77	
Test Method		JEDEC J-STD-020 JESD22-A113		JESD22-A102		EIA/JESD22-A110 EIA/JESD22-A118		JESD22-A104 MIL-STD883 Method 1010.7	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/238	Pass	0f/77	Pass	0f/77	Pass	0f/77	Pass
	Lot2	0f/238	Pass	0f/77	Pass	0f/77	Pass	0f/77	Pass
	Lot3	0f/238	Pass	0f/77	Pass	0f/77	Pass	0f/77	Pass

3.4. Test Conditions & Results - Electrical Test

Electrical Verification Test										
Item	ESD						Latch-Up			
Condition	H.B.M		M.M		CDM		Vtrig		Itrig	
Sample Size	5/case		5/case		5/case		5/case		5/case	
Test Method	EIA/JEDEC JESD22-A114 AEC-Q100-002		EIA/JESD22-A115 AEC-Q100-003		JESD22-C101E		EIA/JESD78 AEC-Q100-004			
Test Results	Result	Comment	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	>2KV	Pass	>200V	Pass	±1KV	Pass	>V_{CC}+1.8V, <V_{SS}-1.8V	Pass	>±200 mA	Pass

4. Estimation of Long-term Failure Rate

4.1. Model

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MTBFmin = $^1/_{\lambda max}$

Where:

λmax = Maximum or worst-case failure rate

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r = Number of failures

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