Reliability Summary Report

Product Type:	1Gb (64Mx16) DDR2
	1Gb (128Mx8) DDR2
Part Number:	KTDM1G2D680BGCEA
	KTDM1G2D680BGIEA
	KTDM1G2D880BGCEA
	KTDM1G2D880BGIEA
Package:	84 ball BGA
	60 ball BGA

1. Features

- JEDEC Standard
- V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V
- Internal pipelined Double-Data-Rate architecture; two data access per clock cycle
- Bi-directional differential data strobe (DQS, $\overline{DQS}$); $\overline{DQS}$ can be disabled for single-ended data strobe operation
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- 8 bank operation
- CAS Latency: 3, 4, 5, 6, 7
- Additive Latency: 0, 1, 2, 3, 4, 5, 6
- Burst Type: Sequential and Interleave
- Burst Length: 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Off-Chip-Driver (OCD) impedance adjustment
- On-Die-Termination for better signal quality
- Special function support
  - 50 / 75 / 150 ohm ODT
  - High Temperature Self refresh rate enable
  - Duty Cycle Corrector
- Auto & Self refresh

2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM1G2D680BGCEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Commercial	Pb-free
KTDM1G2D680BGIEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Industrial	Pb-free
KTDM1G2D880BGCEA	1.8V	DDR2-800 (5-5-5)	60 ball BGA	Commercial	Pb-free
KTDM1G2D880BGIEA	1.8V	DDR2-800 (5-5-5)	60 ball BGA	Industrial	Pb-free

Note:

1. The above description is extracted from the datasheet. Please refer to the document for detailed information.

3. Product Qualification – Die Related Tests

3.1. Test Conditions & Criteria – Die Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	High Temperature Operating Life Test	Ta=125°C V≥1.1Vcc Dynamic	105	0A/1R
2	High Temperature Static Life	Ta=125°C V≥1.1Vcc Static	77	0A/1R
3	High Temperature Bake Test	Ta=150°C	77	0A/1R
4	ESD	HBM	3/case	>±2KV
		MM	3/case	>±200V
5	Latch-Up	Vtrig	3/case	>Vcc+1.8V <Vss-1.8V
		Itrig	3/case	>±200mA

3.2. Test Result – Die Related Tests

No.	Item	Condition	Sample Size	Results (Cumulative Failure)			Comment
				168hrs	500hrs	1000hrs	
1	High Temperature Operating Life Test	Ta=125°C V≥1.1Vcc Dynamic	105	0f/105	0f/105	0f/105	Pass
2	High Temperature Static Life	Ta=125°C V≥1.1Vcc Static	77	0f/77	0f/77	0f/77	Pass
3	High Temperature Bake Test	Ta=150°C	77	-	0f/77	0f/77	Pass
4	ESD	HBM MM CDM	3/case	>±2KV >±200V >±1KV	-	-	Pass
5	Latch-Up	Vtrig	3/case	>2.37V <-1.5V	-	-	Pass
		Itrig		>±200mA			

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4. Product Qualification, Plastic Package Related Tests

4.1. Test Conditions & Criteria – Plastic Package Related Tests

No.	Item	Condition	Sample Size	Accept Criteria
1	Moisture Re-flow Sensitivity	T/C x 5cyc ↓ Bake x 24hrs ↓ Moisture soaking (JEDEC level III) ↓ IR(260°C) Reflow x3	238	0A/1R
2*	Highly Accelerated Temperature and Humidity Stress Test	Ta=130°C RH=85% Vcc=1.1Vcc 33.3 Psia	32	0A/1R
3*	Temperature Cycle Test	-55°C (10min) ↑↓ 125°C (10min) AIR	55	0A/1R
4*	Thermal Shock Test	-55°C (10min) ↑↓ 125°C (10min) LIQUID	55	0A/1R

*Samples are sourced from pre-conditioned process (Bake x 24hr → Moisture soaking (JEDEC level III) → IR Reflow x3)

4.2. Test Results – Plastic Package Related Tests – BGA84 & BGA60

No.	Item	Condition	Sample Size	Results (Cumulative Failure)	Comment
1	Moisture Re-flow Sensitivity (MRS)	T/C x 5cyc ↓ Bake 125°C x 24hrs ↓ Soaking 30°C / RH 60% x192hrs ↓ IR(260°C) Reflow x3	238	0f/238	Pass
2	Highly Accelerated Temperature and Humidity Stress Test (HAST)	Ta=130°C RH=85% Vcc=1.1Vcc 33.3 Psia	32	100hrs 0f/32	Pass
3	Temperature Cycle Test (TC)	-55°C (10min) ↑↓ 125°C (10min) AIR	55	1000cyc 0f/55	Pass
4	Thermal Shock Test (TS)	-55°C (10min) ↑↓ 125°C (10min) LIQUID	55	500cyc 0f/55	Pass

Note: Item 2-4 used samples after MRS flow.

5. ESD Test Data

5.1. Human Body Model (Method: EIA/JESD22-A114)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			|Min (for 3ea)|	|Max (for 3ea)|	
R=1.5KΩ C=100pF	Pin to Vcc (+)	3	> 6000V	> 6000V	
	Pin to Vcc (-)	3	> 4000V	> 6000V	
	Pin to Vss (+)	3	> 6000V	> 6000V	
	Pin to Vss (-)	3	> 6000V	> 6000V	
	Pin to Pin (+)	3	> 6000V	> 6000V	
	Pin to Pin (-)	3	> 5000V	> 6000V	
	Vcc to Vss (+)	3	> 6000V	> 6000V	
	Vcc to Vss (-)	3	> 6000V	> 6000V	

5.2. Machine Model (Method: EIA/JESD22-A115)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			|Min (for 3ea)|	|Max (for 3ea)|	
R=0Ω C=200pF	Pin to Vcc (+)	3	> 450V	> 500V	
	Pin to Vcc (-)	3	> 250V	> 400V	
	Pin to Vss (+)	3	> 350V	> 450V	
	Pin to Vss (-)	3	> 300V	> 450V	
	Pin to Pin (+)	3	> 350V	> 400V	
	Pin to Pin (-)	3	> 300V	> 500V	
	Vcc to Vss (+)	3	> 400V	> 400V	
	Vcc to Vss (-)	3	> 350V	> 400V	

5.3. Non-Socket Charged Device Model (JESD22-C101)

Test Condition	Test Mode	Sample Size	Pass Range In Volts		Remark
			|Min (for 3ea)|	|Max (for 3ea)|	
Non-Socket CDM	±1000V	3	FT Pass	FT Pass	

6. Latch-Up Test Data: for JEDEC-STD-78

Trigger Mode	Test Pin	Sample Size	Latch-Up Triggering Range	
			|Min (for 3ea)|	|Max (for 3ea)|
+VT*	I/P	3	3.6V	3.6V
	I/O		3.6V	3.6V
-VT*	I/P	3	1.8V	1.8V
	I/O		1.8V	1.8V
+IT*	I/P	3	300mA	300mA
	I/O		300mA	300mA
-IT*	I/P	3	300mA	300mA
	I/O		300mA	300mA
Power Transient* (Vcc-Vss)	-	3	3.6V	3.6V

*Latch-up did not occur

7. Estimation of Long-term Failure Rate

7.1. Model

L = Aexp(EA/kT)*exp(-BVcc)
Where:
L: Life time
Ea: Activation energy
B: Voltage acceleration factor
T: Absolute temperature
Vcc: Applied voltage

7.2. Statistical Analysis

$\lambda max = \frac{\chi^2(1-\alpha)}{2t}$ [with df=2(r+1)]

MTBFmin = $^1/_{\lambda max}$

Where:
λmax = Maximum or worst-case failure rate
MTBFmin = Minimum (worst-case) expected MTBF
χ^2 = Chi square distribution
r = Number of failures
df = Degrees of freedon
t = total number of test hours (number of devices x number of hours)
α = Statistical error expected in estimate. For 60% confidence, α = 0.4 or 1-α = 0.6

7.3. Calculation of HTOL Data (KTDM1G2D880BGxEA)

Acceleration Factor: Ea = 0.5eV, B = 7.0 (1/V)
Field Condition: Ta = 55°C, Vcc =1.8V
HTOL (Condition)
Acceleration: A_T (125°C:55°C) = 22.45 times
Av (2.2V:1.8V) = 24.68 times

Estimated failure rate = $\frac{1.83 \text{ x } 10^9}{2 \text{ x } (105 \text{ x } 1000) \text{ x } 22.45 \text{ x } 24.68}$

= 15.75 FIT

Reliability Summary Report

Product Type:	1Gb (64Mx16) DDR2
	1Gb (128Mx8) DDR2
Part Number:	KTDM1G2D680BGAEA
	KTDM1G2D880BGAEA
Package:	84 ball BGA
	60 ball BGA

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1. Features

- JEDEC Standard
- V_{DD} = 1.8V ± 0.1V; V_{DDQ} = 1.8V ± 0.1V
- Internal pipelined Double-Data-Rate architecture; two data access per clock cycle
- Bi-directional differential data strobe (DQS, $\overline{DQS}$); $\overline{DQS}$ can be disabled for single-ended data strobe operation
- On-chip DLL
- Differential clock inputs (CLK and $\overline{CLK}$)
- DLL aligns DQ and DQS transition with CLK transition
- 8 bank operation
- CAS Latency: 3, 4, 5, 6, 7
- Additive Latency: 0, 1, 2, 3, 4, 5, 6
- Burst Type: Sequential and Interleave
- Burst Length: 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READ; center-aligned with data for WRITE
- Data mask (DM) for write masking only
- Off-Chip-Driver (OCD) impedance adjustment
- On-Die-Termination for better signal quality

2. Package Information

Product No.	VDD	Data Rate (CL-tRCD-tRP)	Package	Temperature	Comments
KTDM1G2D680BGAEA	1.8V	DDR2-800 (5-5-5)	84 ball BGA	Automotive	Pb-free
KTDM1G2D880BGAEA	1.8V	DDR2-800 (5-5-5)	60 ball BGA	Automotive	Pb-free

Note:

1. The above description is extracted from the datasheet. Please refer to the document for detailed information.

3. Product Qualification – Die Related Tests

3.1. Test Conditions & Results - Life Test (128Mx8)

Accelerated Life Stress Test									
Item		High Temperature Operating Life Test		Low Temperature Operating Life Test		High Temperature Bake Test		ELFR	
Condition		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = -40°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = 150°C, 1000 hrs		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 72 hrs	
Sample Size		105		105		77		1200	
Test Method		JESD22-A108		JESD22-A108		JESD22-A103		AEC Q100-008	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot2	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot3	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass

3.2. Test Conditions & Results - Life Test (64Mx16)

Accelerated Life Stress Test									
Item		High Temperature Operating Life Test		Low Temperature Operating Life Test		High Temperature Bake Test		ELFR	
Condition		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = -40°C V ≥ 1.1 x Vcc Dynamic, 1000 hrs		Ta = 150°C, 1000 hrs		Ta = 125°C V ≥ 1.1 x Vcc Dynamic, 72 hrs	
Sample Size		105		105		77		1200	
Test Method		JESD22-A108		JESD22-A108		JESD22-A103		AEC Q100-008	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot2	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass
	Lot3	0f/105	Pass	0f/105	Pass	0f/77	Pass	0f/1200	Pass

3.3. Test Conditions & Results - Environmental Test (84 Ball BGA)

Accelerated Environment Stress Test							
Item		Preconditioning		Highly Accelerated Temperature and Humidity Stress Test		Temperature Cycle Test	
Condition		T/C x 5cyc Bake x 24hrs Moisture soaking (JEDEC level III) IR (260°C) Reflow x3		Ta = 130°C RH = 85% Vstress = 1.1 x Vcc 33.3 Psia, 100 hrs		55°C (10min) ~ 125°C (10min), Air to Air, 1000 cycles	
Sample Size		238		32		55	
Test Method		JEDEC J-STD-020 JESD22-A113		EIA/JESD22-A110 EIA/JESD22-A118		JESD22-A104 MIL-STD883 Method 1010.7	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/238	Pass	0f/32	Pass	0f/55	Pass
	Lot2	0f/238	Pass	0f/32	Pass	0f/55	Pass
	Lot3	0f/238	Pass	0f/32	Pass	0f/55	Pass

3.4. Test Conditions & Results - Environmental Test (60Ball BGA)

Accelerated Environment Stress Test							
Item		Preconditioning		Highly Accelerated Temperature and Humidity Stress Test		Temperature Cycle Test	
Condition		T/C x 5cyc Bake x 24hrs Moisture soaking (JEDEC level III) IR (260°C) Reflow x3		Ta = 130°C RH = 85% Vstress = 1.1 x Vcc 33.3 Psia, 100 hrs		55°C (10min) ~ 125°C (10min), Air to Air, 1000 cycles	
Sample Size		238		32		55	
Test Method		JEDEC J-STD-020 JESD22-A113		EIA/JESD22-A110 EIA/JESD22-A118		JESD22-A104 MIL-STD883 Method 1010.7	
Test Results	Lot	Result	Comment	Result	Comment	Result	Comment
	Lot1	0f/238	Pass	0f/32	Pass	0f/55	Pass
	Lot2	0f/238	Pass	0f/32	Pass	0f/55	Pass
	Lot3	0f/238	Pass	0f/32	Pass	0f/55	Pass

3.5. Test Conditions & Results - Electrical Test (84 Ball BGA)

Electrical Verification Test										
Item	**ESD**						**Latch-Up**			
Condition	H.B.M		M.M		CDM		Vtrig		Itrig	
Sample Size	5/case		5/case		5/case		5/case		5/case	
Test Method	EIA/JEDEC JESD22-A114 AEC-Q100-002		EIA/JESD22-A115 AEC-Q100-003		JESD22-C101E		EIA/JESD78 AEC-Q100-004			
Test Results	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**
	>2KV	Pass	>200V	Pass	±1KV	Pass	$>V_{CC}+1.8V$, $<V_{SS}-1.8V$	Pass	>±200 mA	Pass

3.6. Test Conditions & Results - Electrical Test (60 Ball BGA)

Electrical Verification Test										
Item	**ESD**						**Latch-Up**			
Condition	H.B.M		M.M		CDM		Vtrig		Itrig	
Sample Size	5/case		5/case		5/case		5/case		5/case	
Test Method	EIA/JEDEC JESD22-A114 AEC-Q100-002		EIA/JESD22-A115 AEC-Q100-003		JESD22-C101E		EIA/JESD78 AEC-Q100-004			
Test Results	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**	**Result**	**Comment**
	>2KV	Pass	>200V	Pass	±1KV	Pass	$>V_{CC}+1.8V$, $<V_{SS}-1.8V$	Pass	>±200 mA	Pass

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4. Estimation of Long-term Failure Rate

4.1. Model

L = Aexp(EA/kT)*exp(-BVcc)
Where:
L: Life time
Ea: Activation energy
B: Voltage acceleration factor
T: Absolute temperature
Vcc: Applied voltage

4.2. Statistical Analysis

$$\lambda\text{max} = \frac{\chi^2(1-\alpha)}{2t}$$ [with df=2(r+1)]

MTBFmin = $^1/_{\lambda\text{max}}$

Where:
λmax = Maximum or worst-case failure rate
MTBFmin = Minimum (worst-case) expected MTBF
χ^2 = Chi square distribution
r = Number of failures
df = Degrees of freedon
t = total number of test hours (number of devices x number of hours)
α = Statistical error expected in estimate. For 60% confidence, α = 0.4 or 1-α = 0.6

4.3. Calculation of HTOL Data

Acceleration Factor: Ea = 0.5eV, B = 7.0 (1/V)
Field Condition: Ta = 55°C, Vcc =1.8V
HTOL (Condition)
Acceleration: A_T (125°C:55°C) = 22.45 times
Av (2.2V:1.8V) = 24.68 times

Estimated failure rate = $\frac{1.83 \text{ x } 10^9}{2 \text{ x } (315 \text{ x } 1000) \text{ x } 22.45 \text{ x } 24.68}$

= 5.25 FIT