SMARTsemi
Memory IC Datasheet

Industrial Grade eMMC 153b

REVISION HISTORY

Date	Revision	Section(s)	Description
April 2024	1.0	All	Initial Release

ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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FEATURES

- **Capacity**
  - 128GB
- **Electrical/Physical Interface**
  - Compliant with eMMC Specification Version 5.1
  - 153 Ball FBGA Package
- **Bus Mode[1]**
  - High-speed eMMC protocol
    - SDR52, DDR52, HS200, and HS400
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1-bit command, 8-bit data bus) and a hardware reset
- **Bus Width**
  - 1-bit, 4-bit, 8-bit
- **Performance (HS400)**
  - Read:
    - Up to 330 MB/s
  - Write:
    - Up to 140 MB/s
- **Operating Temperature[2]**
  - Industrial grade: -40°C to +85°C
- **Storage Temperature[2]**
  - -40°C to +85°C
- **Input Power:**
  - V_{CC}: 2.7 – 3.6V
  - V_{CCQ} (Dual voltage): 1.7 – 1.95V or 2.7 – 3.6V
- **Power Consumption (HS400, I_{CC}/I_{CCQ})**
  - Read: 125/170mA
  - Write: 110/85mA
  - Standby: 30/170µA
- **Certification & Compliance**
  - RoHS

- **NAND Technology**
  - TLC
- **Reliability**
  - Configurable error correction code (ECC)
  - Bad block management
  - Wear leveling
  - Garbage collection
- **Security**
  - Trim, Erase
  - Secure Write Protection
- **Additional Features**
  - Field firmware update (FFU)
  - Production state awareness (PSA)
  - Replay Protected Memory Block (RPMB)
  - High Priority Interrupt (HPI)
  - Command Queuing
  - Cache flushing report
  - Cache barrier

NOTES:
[1] HS200 and HS400 modes are supported only when V_{CCQ} is in 1.7 – 1.95V.
[2] Ambient temperature.

GENERAL DESCRIPTION

Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMART's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

Functional Block Diagram

eMMC Block Diagram

PERFORMANCE

Performance Characteristics

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
128 GB	330	140	16000	6500

Capacity	HS200 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
128 GB	190	115	10000	4300

Capacity	DDR52 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
128 GB	95	65	8200	4600

1. *Performance measured based on the internal tool.*
2. *Write Cache is on.*

ENDURANCE

Drive Lifetime[1]

Capacity	Value (Max)
128GB	129 TBW

1   Endurance is related directly to the User Specific Workload. Measured with 100% Sequential Workload.

RELIABILITY

Failure rate

Parameter	Value
FIT @ Tc = 40°C	136

Data Retention

Parameter	Value
Data Retention (@ 55°C)	10 years when 90% life remaining
	1 year when 10% life remaining

Operating and Storage Temperature[1]

Parameter	Value
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +85°C

[1] Operating temperature herein is Ambient Temperature.

POWER CONSUMPTION

Condition1		ICC/ICCQ (Typical)	Units
		128GB (native)	
Write	DDR52	85/75	mA
	HS200	105/85	mA
	HS400	110/85	mA
Read	DDR52	50/110	mA
	HS200	95/120	mA
	HS400	125/170	mA
Sleep current		130	µA
Standby		30/170	µA

1. Bus in x8 I/O mode; 25°C; VCCQ = 1.8 V in HS200 and HS400. Measurements done as maximum RMS current consumption over 100 milliseconds.

ELECTRICAL SPECIFICATION

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is the supply voltage for controller and Flash memory power; V_{CCQ} is the supply voltage for controller and eMMC I/O voltage.

Power Connections

Power Requirements

Symbol	Parameter	Value (Minimum)	Value (Typical)	Value (Maximum)	Unit
V_{CC}	Voltage supply to Flash memory	2.7	3.3	3.6	V
V_{CCQ}	Voltage supply to host interface	2.7 (high range) 1.70 (low range)	3.3 (high range) 1.80 (low range)	3.6 (high range) 1.95 (low range)	V
V_{DDi}	Internal voltage regulator connection to external capacitor	-	-	-	-

Recommended eMMC Connection

Capacitor and Resistor Specifications

Parameter	Symbol	Min	Max	Typ	Units	Remark
Pull-up resistance for CMD	R_CMD	4.7	50	10	Kohm	to prevent bus floating
Pull-up resistance for DAT0 ~ 7	R_DAT	10	50	10	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	10	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Pull-down resistance for Data Strobe	R_DS	10	50	10	Kohm	
Impedance on CLK / CMD / DAT0~7		45	55	50	ohm	Impedance match
Serial's resistance on CLK line	SR_CLK	-	-	0	ohm	If customer want to put serial resistance except 0 ohm, they need to check timing are all in SPEC.
Serial's resistance on power trace	R_VCC R_VCCQ	-	-	0	ohm	Typeical size 0603 or 0805.
Serial's resistance on CMD / DAT0~7 line / RST_n / RCLK	SR_RST_n SR_DS SR_CMD SR_DAT0~7	-	-	0	ohm	If customer want to put serial resistance except 0 ohm, they need to check timing are all in SPEC.
V_{ccQ} capacitor value	C1	2.2	4.7	4.7	μF	Coupling capacitor should be connected with VDDQ and VSSQ as closely as possible
	C2	0.1	0.22	0.1	μF	
	CH1	1	2.2	1	μF	CH1 should be placed adjacent to VccQ-VssQ balls (#C6 and #C4 accordingly, next to DAT[7..0] balls), It should be located as close as possible to the balls defined in order to minimize connection parasitics.
V_{cc} capacitor value	C3	2.2	4.7	4.7	μF	Coupling capacitor should be connected with VDD and VSS as closely as possible
	C4	0.1	0.22	0.22	μF	
VDDi capacitor value (C_{RBI})	C5	1	4.7	2.2	μF	Coupling capacitor should be connected with VDDi and VSSi as closely as possible
	C6	0.1	0.22	0.1	μF	
Vendor Specific	TP1~7	-	-	-	-	The function of these signals is defined and specified by the controller vendor. A pin that is not to be used in normal applications and that may or may not have an internal connection. The VSF signals shall be treated as NU signals by the user. The VSF signals shall reserved test points on the PCB, avoid reference high speed layer and power plane.

Note: It doesn't matter to put Pull-up resistors and Serial's resistors closer to host or eMMC. However, it's recommended to put all resistors on the same PCB side. (Top or Bottom)

MECHANICAL SPECIFICATION

153-Ball BGA Dimensions – 11.5 mm x 13 mm x 1 mm

	SYM.	DIMENSION (mm)		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.95	1.00
STAND OFF	A1	0.17	0.22	0.27
SUBSTRATE THICKNESS	A2	—	0.18	—
MOLD THICKNESS	A3	—	0.55	—
BALL WIDTH	b	0.25	0.30	0.35
BODY SIZE	D	12.90	13.00	13.10
BALL DIAMETER (PRE-REFLOW)			0.30	
BALL OPENING			0.275	
EDGE BALL CENTER TO CENTER	D1		6.50 BSC	
BODY SIZE	E	11.40	11.50	11.60
EDGE BALL CENTER TO CENTER	E1		6.50 BSC	
BODY CENTER TO CONTACT BALL	SD		0.25 BSC	
	SE		0.25 BSC	
JEDEC(REF)			MO-276(REF.)	
BALL PITCH	e		0.50 BSC	
BALL COUNT	N		153	
TEST PAD	TE	0.25	0.30	0.35
TEST PAD	TD	0.25	0.30	0.35
PACKAGE EDGE TOLERANCE	aaa		0.15	
MOLD FLATNESS	bbb		0.20	
COPLANARITY	ddd		0.08	
BALL OFFSET(PACKAGE)	eee		0.15	
BALL OFFSET(BALL)	fff		0.05	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.

Mechanical Dimensions

Parameter	Value
Length	13.00 mm
Width	11.50 mm
Height	1.00 mm

Recommended Reflow Profiles

Parameter	Value
Peak Temperature	235 - 245°C
Time Above liquidus	45 to 70 seconds
Cooling Rate	< 4°C/sec

Note: Each solder paste manufacturer will have their own reflow profile specification. It's recommended customers follow the solder paste manufacturer's reflow profile specification and optimize the reflow profile based on product complexity for the assembly process.

Rev: 1.0
DS881

EMMC BALL-OUT DIAGRAM

Figure 1 153-Ball Pin Assignments (Top View, Balls Down)*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDi	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		VCC				VSF		NC	NC	NC	F
G	NC	NC	RFU		VSS				VSF		NC	NC	NC	G
H	NC	NC	NC		DS				VSS		NC	NC	NC	H
J	NC	NC	NC		VSS				VCC		NC	NC	NC	J
K	NC	NC	NC	RST_n	RFU	RFU	VSS	VCC	VSF		NC	NC	NC	K
L	NC	NC	NC								NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	RFU	NC	NC	VSF	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Pinout Descriptions

Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock Signal.
RST_n	Input	Hardware Reset Signal.
CMD	I/O	Command Signal.
DAT[7:0]	I/O	Data Bus.
DS	Output	Data Strobe Signal, Used in HS400 mode.
V_{CC}	Supply	Supply voltage for controller and Flash memory power.
V_{CCQ}	Supply	Supply voltage for controller and eMMC I/O power.
V_{SS}	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
V_{SSQ}	Supply	Supply voltage ground for controller and IO Flash memory. Can be short with VSS.
V_{DDi}		Connect capacitor from VDDi to GND for stabilize internal power.
NC	-	In eMMC chip is no connect. Left it floating.
RFU	-	Reserved for future use. Left it floating for future use.
VSF	-	Vendor Specific Function. Reserved for test points on the PCB, default NU (Not Used)

Note: A6 VSS, J5 VSS, H5 DS could be floated to achieve eMMC 4.5 force conversion.

REGISTERS

Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

CID Register Field Parameters

CID Fields Name	Field	Width	CID slice	Value
Manufacturer ID	MID	8	[127:120]	0xF6
Reserved	-	6	[119:114]	--
Device/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x00
Product name	PNM[1]	48	[103:56]	DGP3C∆ 0x444750334320
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN[2]	32	[47:16]	--
Manufacturing date	MDT[3]	8	[15:8]	--
CRC7 checksum	CRC	7	[7:1]	--
Reserved	-	1	[0:0]	--

(1) The product name, PNM is a string, 6 ASCII characters long and " ∆" is a space(0x20).

(2) Unique for each device. 32-bit unsigned binary integer.

(3) 2 hex digits for device manufacturing month and year.

OCR Register Field Definitions

VDD Voltage Window	Width (Bits)	OCR Bits	OCR Value
Ready/Busy	1	[31]	card power up status bit (busy)(1)
Access Mode	2	[30:29]	10b
Reserved	5	[28:24]	--
2.7-3.6V	9	[23:15]	1 1111 1111b
2.0-2.6V	7	[14:8]	000 0000b
1.70-1.95V	1	[7]	1b
Reserved	7	[6:0]	--

Note:

(1) This bit is set to low if the device has not finished the power up routine.

CSD Register Field Parameters

Name	Field	Width (Bits)	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	[127:126]	0x03
System specification version	SPEC_VERS	4	[125:122]	0x04
Reserved	--	2	[121:120]	--
Data read access time 1	TAAC	8	[119:112]	0x4F
Data read access time 2 in CLK cycles (NSAC x 100)	NSAC	8	[111:104]	0x01
Maximum bus clock frequency	TRAN_SPEED	8	[103:96]	0x32
Device command classes	CCC	12	[95:84]	0x8F5
Maximum read data block length	READ_BL_LEN	4	[83:80]	0x09
Partial blocks for reads supported	READ_BL_PARTIAL	1	[79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0x00
DSR implemented	DSR_IMP	1	[76]	0x00
Reserved	--	2	[75:74]	--
Device size	C-SIZE	12	[73:62]	0xFFF
Maximum read current as VDD,min	VDD_R_CURR_MIN	3	[61:59]	0x07
Maximum read current as VDD,max	VDD_R_CURR_MAX	3	[58:56]	0x07
Maximum write current as VDD,min	VDD_W_CURR_MIN	3	[55:53]	0x07
Maximum write current as VDD,max	VDD_W_CURR_MAX	3	[52:50]	0x07
Device size multiplier	C-SIZE_MULT	3	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	[31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0x00
Write-speed factor	R2W_FACTOR	3	[28:26]	0x02
Maximum write data block length	WRITE_BL_LEN	4	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0x00

Name	Field	Width (Bits)	CSD Bits	CSD Value
Reserved	-	4	[20:17]	--
Content protection application	CONTENT_PROT_APP	1	[16]	0x00
File-format group	FILE_FORMAT_GRP	1	[15]	0x00
Copy flag (OTP)	COPY	1	[14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0x00
Temporary write protection	TEMP_WRITE_PROTECT	1	[12]	0x00
File format	FILE_FORMAT	2	[11:10]	0x00
ECC code	ECC	2	[9:8]	0x00
CRC	CRC	7	[7:1]	--
Not used; always 1	-	1	[0]	0x01

ECSD Register Field Parameters

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Reserved	--	6	-	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported command sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3C
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x20
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x03
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x53

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES	1	R	[493]	0x01
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0xFFFFFFFF
Reserved	-	181	-	[486:306]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00000000
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x0000
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x01
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device Version	Device version	2	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0x01
Power class for200MHz · DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0xEE
Cache size	CACHE_SIZE	4	R	[252:249]	0x00000600
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x43
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x28
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00000000

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x0B
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x17
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x14
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x10
Sector count[1]	SEC-COUNT	4	R	[215:212]	0x0E8F8000
Reserved	-	1	-	[211]	--
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x08
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x14
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x08
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x14
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x08
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x0F
Reserved	-	1	-	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x77
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x77
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x0B

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x25
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card type	CARD_TYPE	1	R	[196]	0x57
Reserved	-	1	-	[195]	--
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	-	1	-	[193]	--
Extended CSD revision	EXT_CSD_REV	1	-	[192]	0x08
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	-	1	-	[190]	--
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	-	1	-	[188]	--
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	-	1	-	[186]	--
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved	-	1	-	[184]	--
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved	-	1	-	[182]	--
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved	-	1	-	[180]	--
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved	-	1	-	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	0x00
Reserved	-	1	-	[172]	--
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	-	1	-	[170]	--
Firmware configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x15
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
Hardware reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT	1	R/W/E, R/W/E_P	[160]	0x07
Maximum enhanced area size[1]	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x00136A
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning setting	PARTITIONING_SETTING-COMPLETED	1	R/W	[155]	0x00
General-purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00

Name	Field	Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x000000
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	0x00000000
Reserved	-	1	-	[135]	--
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved	-	2	-	[129:128]	--
Vendor specific fields	VENDOR_SPECIFIC_NFIELD	64	<vs>	[127:64]	0x00
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 command control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved	-	2	-	[28:27]	--
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATASIZE	4	R	[21:18]	0x04D8C000
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x01
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x39
Reserved	-	16	-	[15:0]	--

NOTES:

1. Obsolete values should be don't care.
2. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing (see Section 10.6.1 of JESD84-B50). If the host sets value 2 the Device changes its timingto HS200 interface timing (see Section 10.8.1 of JESD84-B50), If the host sets HS_TIMING[3:0] to 0x3,the device changes its timing to HS400 interface timing (see10.10).
3. It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.
4. The values of Device version, Cache size, Sector Count, Max Enhanced Area Size, Enhanced User Data Area Size and Max pre loading data size are expressed in Decimal, while the value of h is the abbreviationof Hexadecimal.

PART NUMBERS

Part Number	Operating temperature	Capacity
KTMDGP3CTI01	-40°C to 85°C	128GB

KTMDGP3CTI01

April 2024

PART NUMBER DECODER

KT **M** **xG** **P3C** **T** **x** **0** **1**

SMART Semiconductor

Product Type

Disk Capacity

Controller Assembly Version

Flash Identifier

Operating Temp Range

Configuration

Firmware Version

1: Initial release

Binary capacity: DG: 128GB

Vendor Flash

0: Default config.

M: eMMC 153-ball (11.5x13mm)

I: -40°C to 85°C

Vendor Controller

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