SMARTsemi
Memory IC Datasheet

Extended Temperature eMMC 153b

June 2025

Rev 1.0

Doc: DS1011

REVISION HISTORY

Date	Revision	Section(s)	Description
June 2025	1.0	All	Initial Release

ESD Caution – Handling
Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1 GENERAL DESCRIPTION

1.1 Overview

SMARTsemi's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMARTsemi's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, Global wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMARTsemi's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

1.2 Features

- Industrial Standard Interface
  - JEDEC / eMMC Standard Version 5.1 Compliant

- eMMC 5.1 Enhanced Features
  - 12-signal interface (including CMD, CLK, DS, DAT[7:0], and RST_n)
  - Programmable bus width: 1-bit, 4-bit, and 8-bit
  - Supports HS400 high speed interface timing mode
  - Up to 200MHz clock frequency
  - Supports eMMC Field firmware update (FFU)
  - Supports eMMC production state awareness (PSA)
  - Supports eMMC device health report
  - Supports Boot Feature and Boot Partition
  - Replay Protected Memory Block (RPMB)
  - Trim, Sanitize, Discard, Secure Erase
  - High Priority Interrupt (HPI)
  - Background Operations, Garbage Collection and Wear Leveling
  - Reliable Write
  - Supports Command Queuing
  - Supports Enhanced Strobe in HS400 Mode
  - Supports eMMC Background Operation Control
  - Supports Lock/Unlock
  - Supports Secure Removal Type
  - Supports Configurable Drive Strength
  - Supports Write protect, Secure Write Protection
  - Supports Cache, Cache Barrier, Cache Flushing Report
  - Hardware/ Software Reset
  - Supports PON, Sleep/Awake

- Robust Data Protection and Endurance
  - Configurable ECC engine with zero overhead pipeline greatly reduces data loss rates and increases data endurance
  - Static data refresh and early block failure monitoring/retirement ensure the data reliability
  - Power loss detection and mapping table auto-rebuild algorithm support power-down data protection
  - Global wear leveling maximizes product lifespan with minimal wear leveling and write amplification overhead

- Supply Voltage
  - eMMC Interface Power (VCC): 3.3V
  - eMMC I/O Power (VCCQ): 3.3V or 1.8V
- Multiple Densities and Packages
  - Available in 64GB/128GB/ TLC mode density
  - 153-ball standard FBGA packages
  - Green Package, REACH and RoHS Compliant
- Operating Temperature
  - Extended Temperature: -25°C ~ +85°C

2 OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1 Performance

Table 1: Performance Table

TLC Partition Burst Performance

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
64GB	330	230	13400	4300
128GB	330	200	9547	2374

(1) Test condition: Bus in x8 I/O, HS400 mode. Write cache off.

2.2 Power Consumption

Table 2: Current Consumption

Condition		I_{CC}/I_{CCQ} (V_{CCQ}=1.8V/V_{CC}=3.3V)		Units
		64GB	128GB	
Write	HS400	70/65	70/105	mA
Read	HS400	155/100	155/105	mA
Idle		0.15/0.06	0.15/0.07	mA

2.3 Data Reliability

- **Static and Dynamic Wear Leveling:** This feature eliminates overstressing Flash media by spreading the data writes across all Flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.
- **ECC**: Utilize LDPC ECC to provide correction of user data.
- **Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

2.4 Failure Rate

Table 3: Failure Rate

Failure Rate	64GB	128GB
FIT @ Tc = 40°C	116.73	138.52

2.5 Environmental Conditions

Table 4: Environmental Conditions and Test Conditions

Parameter	Value
Operating Temperature – Extended Temperature	-25°C to 85°C
Storage Temperature	-40°C to 85°C

2.6 Endurance

Table 5: Reliability Characteristics

Item		Value	
Data Retention (@40˚C)		5 years when 90% life remaining	
		1 year when 10% life remaining	
TLC mode Endurance[1]	64 GB	100% Sequential Workload	168 TBW
	128 GB		336 TBW

[1] Endurance is directly related to the user specific workload.

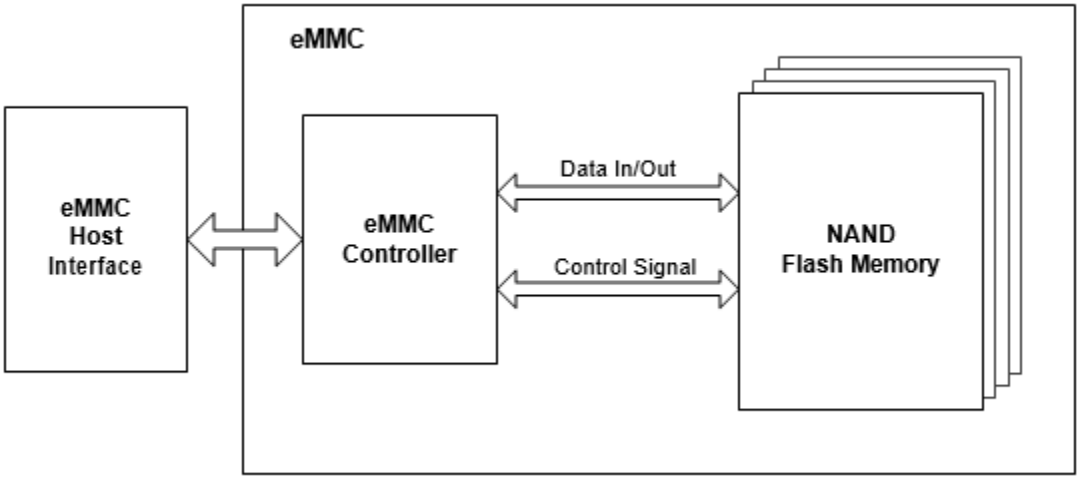
[2] Reference from JESD218

3 PRODUCT DESCRIPTION

The eMMC device includes NAND Flash Memory paired with an intelligent embedded MMC controller which runs advanced firmware to manage the NAND media and utilizes the industry standard eMMC interface for easy device integration into any system using a processor with an MMC host.

3.1 Functional Block Diagram

Figure 1: eMMC Block Diagram



4 PACKAGE INFORMATION

4.1 Signal Interface

4.1.1 eMMC Ball-out Diagram

Figure 2: 153-Ball Pin Assignments (Top View, Balls Down)*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDDi	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		VCC					VSF		NC	NC	NC	F
G	NC	NC	RFU		VSS					VSF		NC	NC	NC	G
H	NC	NC	NC		DS					VSS		NC	NC	NC	H
J	NC	NC	NC		VSS					VCC		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	VSS	VCC	VSF		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	RFU	NC	NC	VSF	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

4.1.2 Signal Descriptions

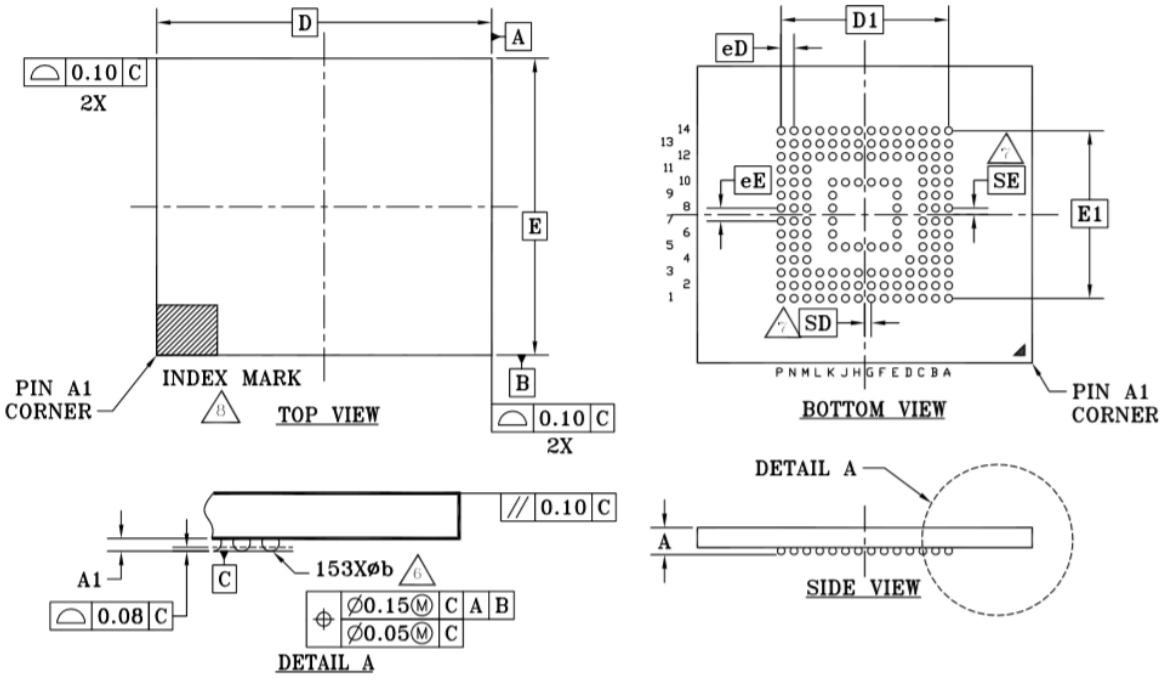
Table 6: Signal Descriptions

Signal	Type	Description
CLK	Input	Clock Signal.
DS	Output	Data Strobe Signal, Used in HS400 mode.
CMD	I/O	Command Signal.
DAT0 – DAT7	I/O	Data Bus.
RST_n	Input	Hardware Reset Signal.
VCC	Supply	Supply voltage for controller and Flash memory power.
VCCQ	Supply	Supply voltage for controller and eMMC I/O power.
VSS	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
VSSQ	Supply	Supply voltage ground for controller and IO Flash memory. Can be short with VSS.
VDDi	-	Connect capacitor from VDDi to GND for stabilize internal power.
NC	-	In eMMC chip is no connect. Left it floating.
RFU	-	Reserved for future use. Left it floating for future use.
VSF	-	Vendor Specific Function. Reserved for test points on the PCB, default NU (Not Used, Float NC)

5 eMMC MECHANICAL SPECIFICATIONS

5.1 Package Dimensions

Figure 3: 153-Ball BGA Dimensions – 11.5 mm x 13 mm x 1.0 mm



PACKAGE	TBD 153			NOTE
JEDEC	MO-276			
D X E	13.00mm X 11.50mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.00	PROFILE
A1	0.17	---	---	BALL HEIGHT
D	13.00 BSC			BODY SIZE
E	11.50 BSC			BODY SIZE
D1	6.50 BSC			MATRIX FOOTPRINT
E1	6.50 BSC			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	153			BALL COUNT
ø b	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC			SOLDER BALL PLACEMENT
	D5-D11,E11-K11,L4-L11,E4-K4 F6-F9,G6-G9,H6-H9,J6-J9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP 95, SECTION 4.6.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP 95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW D OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = e/2
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
9. TEST PADS MAY BE PRESENT BUT ARE NOT SHOWN. THEY ARE FOR INTERNAL USE ONLY AND ARE NOT SOLDER BALLS.

5.2 Recommended Reflow Profiles

Table 7: Recommended Reflow Profile

Reflow Parameters	Suggested Range
Peak Temperature	235 - 245°C
Time Above liquidus	45 to 70 seconds
Cooling Rate	< 4°C/sec

Note: Each solder paste manufacturer will have their own reflow profile specification. It's recommended customers follow the solder paste manufacturer's reflow profile specification and optimize the reflow profile based on product complexity for the assembly process.

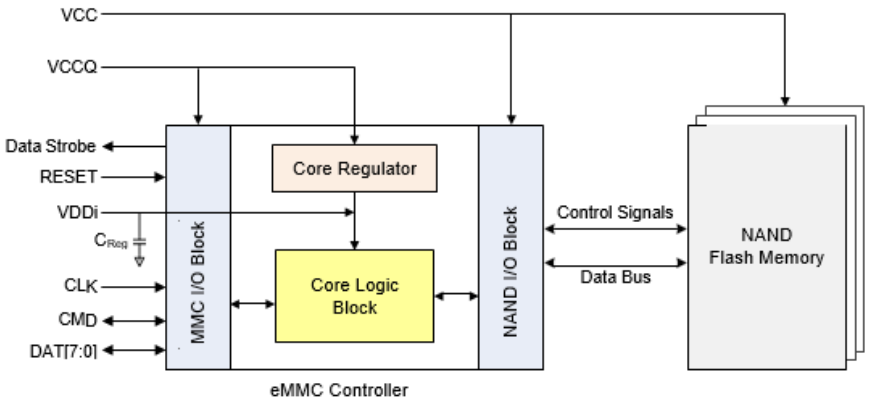
6 ELECTRICAL SPECIFICATION

6.1 Electrical Interface

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is used for the NAND Flash device; V_{CCQ} is used for the controller and the eMMC interface voltage.

Figure 4: System Architecture



6.2 DC Specifications

Table 8: Power Requirements

Symbol	Parameter	Value (Minimum)	Value (Typical)	Value (Maximum)	Unit
V_{CC}	Voltage supply to Flash memory	2.7	3.3	3.6	V
V_{CCQ}	Voltage supply to host interface	1.70 2.7	1.80 3.3	1.95 3.6	V
V_{DDi}	Internal voltage regulator connection to external capacitor	-	-	-	-

Figure 5: Recommended eMMC Connection

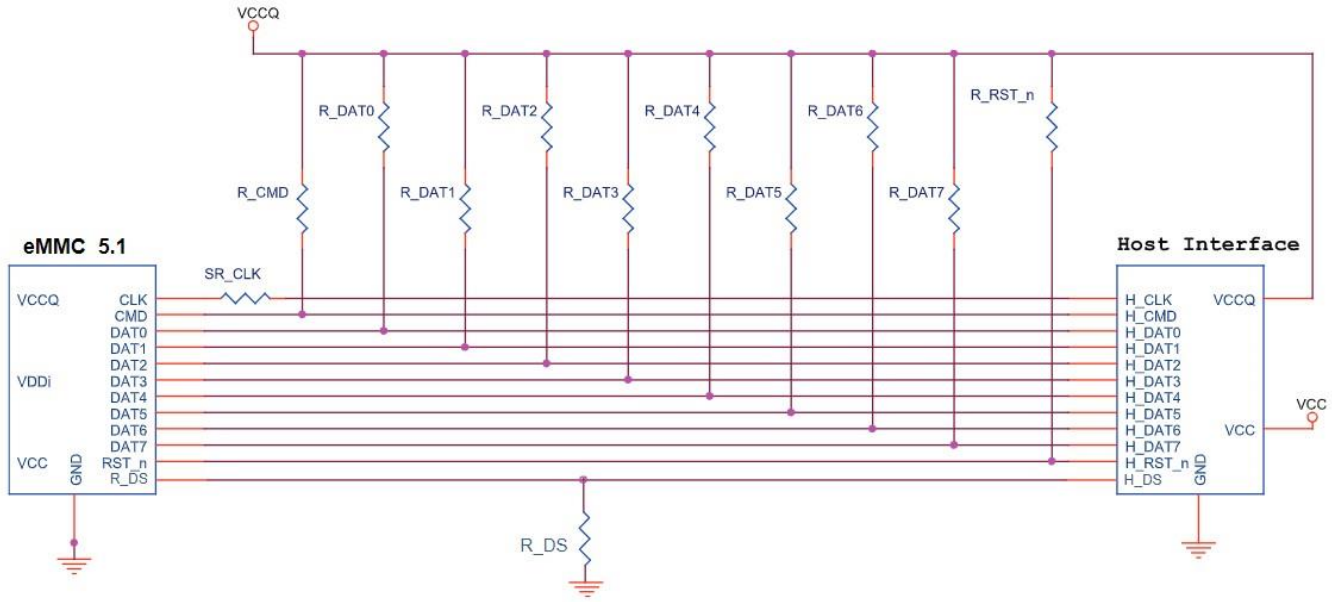


Table 9: Recommended Capacitor and Resistor

Parameter	Symbol	Recommended	Comments
Pull-up resistance for CMD	R_CMD	10 kΩ	To prevent bus floating.
Pull-up resistance for DAT[7:0]	R_DAT	50 kΩ	To prevent bus floating.
Pull-up resistance for RST_n	R_RST_n	50 kΩ	A pull-up resistance on the RST_n (H/W reset) line is not required if the host does not enable the H/W reset feature.
Series termination for CLK	SR_CLK	22Ω	To stabilize the clock signal. It is recommend for customers to perform simulations using the controller IBIS model to confirm this value.
Pull-Down resistance for Data Strobe	R_DS	50 kΩ	

Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.
- Recommended Value and Quantity:
  VCCQ: More than 0.1 µF x 1, 2.2 µF x 1 (for BGA153, this cap should be as close as possible to C6 ball), and 1 x 1 µF
  VCC: More than 0.1 µF x 1 and 2.2 µF x 1
  VDDi: More than 0.1 µF x 1 and 2.2 µF x 1
  A minimum of 1uF is required for VCCQ, VCC, and VDDi.

Place all of the caps shown above. The VCCQ caps should be located as close as possible to the VCCQ/VSSQ balls near the DAT0-7 signals.

7 REGISTER

The registers used in the SMART eMMC are shown in the table below. These registers are described in the sections that follow:

Table 10: Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

* The values in each register are based on TLC configuration.

7.1 CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 11: CID Register Field Parameters

Name	Field	Width (Bits)	CID Bits	SMART CID Value	
Manufacturer ID	MID	8	[127:120]	F6h	
Reserved	-	6	[119:114]	--	
Device / BGA	CBX	2	[113:112]	1h	
OEM/application ID	OID	8	[111:104]	00h	
Product name	PNM	48	[103:56]	64GB	CGP4AΔ (Note4) 0x434750344120
				128GB	DGP4AΔ (Note4) 0x444750344120
Product revision	PRV	8	[55:48]	10h	
Product serial number	PSN	32	[47:16]	(Note 1)	
Manufacturing date	MDT	8	[15:8]	(Note 2)	
CRC7 checksum	CRC	7	[7:1]	(Note 3)	
reserved	-	1	0	01h	

Notes:

1 Unique for each device. 32-bit unsigned binary integer.
2 2 hex digits for device manufacturing month and year.
3 CRC for CID register. Different for each device.
4 The product name uses ASCII code and Δ is space.

7.2 OCR Register

The card identification (OCR) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by the eMMC protocol. Each device is created with a unique identification number.

Table 12: OCR Register Field Definitions

V_{DD} Voltage Window	Width (Bits)	OCR Bits	OCR Value
Ready/Busy	1	[31]	card power up status bit (busy)(1)
Access Mode	2	[30:29]	10b
Reserved	5	[28:24]	--
2.7-3.6V	9	[23:15]	1 1111 1111b
2.0-2.6V	7	[14:8]	000 0000b
1.70-1.95V	1	[7]	1b
Reserved	7	[6:0]	--

Note:

(1) This bit is set to low if the device has not finished the power up routine.

7.3 CSD Register

The card-specific data (CSD) register provides information about accessing the device contents. The CSD register defines the data format, error correction type, maximum data access time, and data transfer speed, as well as whether the DS register can be used. The programmable part of the register (entries marked with W or E in the following table) can be changed by the PROGRAM_CSD (CMD27) command.

Table 13: CSD Register Field Parameters

Name	Field	Width (Bits)	CSD Bits	CSD Value
CSD structure	CSD_STRUCTURE	2	[127:126]	3h
System specification version	SPEC_VERS	4	[125:122]	4h
Reserved	--	2	[121:120]	—
Data read access time 1	TAAC	8	[119:112]	4Fh
Data read access time 2 in CLK cycles (NSAC x 100)	NSAC	8	[111:104]	01h
Maximum bus clock frequency	TRAN_SPEED	8	[103:96]	32h

Name	Field	Width (Bits)	CSD Bits	CSD Value
Device command classes	CCC	12	[95:84]	8F5h
Maximum read data block length	READ_BL_LEN	4	[83:80]	9h
Partial blocks for reads supported	READ_BL_PARTIAL	1	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	[77]	0h
DSR implemented	DSR_IMP	1	[76]	0h
Reserved	--	2	[75:74]	—
Device size	C-SIZE	12	[73:62]	FFFh
Maximum read current as VDD,min	VDD_R_CURR_MIN	3	[61:59]	7h
Maximum read current as VDD,max	VDD_R_CURR_MAX	3	[58:56]	7h
Maximum write current as VDD,min	VDD_W_CURR_MIN	3	[55:53]	7h
Maximum write current as VDD,max	VDD_W_CURR_MAX	3	[52:50]	7h
Device size multiplier	C-SIZE_MULT	3	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	[30:29]	0h
Write-speed factor	R2W_FACTOR	3	[28:26]	2h
Maximum write data block length	WRITE_BL_LEN	4	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	[21]	0h
Reserved	--	4	[20:17]	—
Content protection application	CONTENT_PROT_APP	1	[16]	0h
File-format group	FILE_FORMAT_GRP	1	[15]	0h
Copy flag (OTP)	COPY	1	[14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	[13]	0h
Temporary write protection	TEMP_WRITE_PROTECT	1	[12]	0h
File format	FILE_FORMAT	2	[11:10]	0h
ECC code	ECC	2	[9:8]	0h
CRC	CRC	7	[7:1]	--
Not used; always 1	--	1	[0]	Always 1

7.4 ECSD Register

The 512-byte extended card-specific data (ECSD) register defines device properties and selected modes. The most significant 320 bytes are the properties segment. This segment defines device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. The modes segment defines the configuration in which the device is working. The host can change the properties of modes segments using the SWITCH command.

Table 14: ECSD Register Field Parameters

Name	Field	Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Reserved	--	6	--	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported command sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3C
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x20
Data tag support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE	1	R	[498]	0x03
Tag resources size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	64GB: 0x29 128GB: 0x53
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES	1	R	[493]	0x01
FFU features	FFU_FEATURES	1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00
FFU Argument	FFU_ARG	4	R	[490:487]	0x0000FFFF
Reserved	--	181	--	[486: 306]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	N/A
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	Variable

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	Variable
Pre EOL information	PRE_EOL_INFO	1	R	[267]	Variable
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x01
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x01
Device Version	Device version	2	R	[263:262]	0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0x0000000000000004
Power class for200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x600
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x32
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0xFF
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x64
Reserved	--	1	--	[240]	--
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200 MHz at 1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200 MHz at 1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved	--	1	--	[233]	--
TRIM multiplier	TRIM_MULT	1	R	[232]	0x05
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
SECURE ERASE multiplier	SEC_ERASE_MULT	1	R	[230]	0xF7
SECURE TRIM multiplier	SEC_TRIM_MULT	1	R	[229]	0xF7

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved	--	1	--	[227]	--
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20
Access size	ACC_SIZE	1	R	[225]	0x08
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_ MULT	1	R	[223]	0x05
Reliable write-sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10
Sleep current (V_{CC})	S_C_VCC	1	R	[220]	0x08
Sleep current (V_{CCQ})	S_C_VCCQ	1	R	[219]	0x08
Production state awareness timeout	PRODUCTION_STATE_AWARENESS _TIMEOUT	1	R	[218]	0x14
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x15
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x0F
Sector count	SEC-COUNT	4	R	[215:212]	64GB: 0x747C000
					128GB: 0xE8F8000
Reserved	--	1	--	[211]	--
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0x08
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0x08
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x08
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x08
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0x08
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0x08
Reserved	--	1	--	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0xFF
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0xFF
I/O driver strength	DRIVER_STRENGTH	1	R	[197]	0x1F
Card type	CARD_TYPE	1	R	[196]	0x57
Reserved	--	1	--	[195]	--
CSD structure version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	--	1	--	[193]	--
Extended CSD revision	EXT_CSD_REV	1	--	[192]	0x08
Command set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved	--	1	--	[190]	--
Command set revision	CMD_SET_REV	1	R	[189]	0x00
Reserved	--	1	--	[188]	--
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved	--	1	--	[186]	--
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved	--	1	--	[184]	--
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved	--	1	--	[182]	--
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved	--	1	--	[180]	--
Partition configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved	--	1	--	[176]	--
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protection register	BOOT_WP	1	R/W, R/W/C_P	[173]	0x00

Name	Field	Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Reserved	--	1	-	[172]	--
User write protection register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	--	1	--	[170]	--
Firmware configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x00
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x15
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
Hardware reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT	1	R/W/E, R/W/E_P	[160]	0x07
Maximum enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	64GB: 0x9B5 128GB: 0x136A
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning setting	PARTITIONING_SETTING-COMPLETED	1	R/W	[155]	0x00
General-purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced user data start address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved	-	1	-	[135]	--
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved	-	2	-	[129:128]	--

Name	Field	Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Vendor specific fields	VENDOR_SPECIFIC_NFIELD	64	<vs>	[127:64]	0x00
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 command control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL	1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00
Reserved	-	2	-	[28:27]	--
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING_DATASIZE	4	R	[21:18]	64GB: 0x026B1000 128GB: 0x04D62000
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x01
Secure removal type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x01
Reserved	-	16	-	[15:0]	--

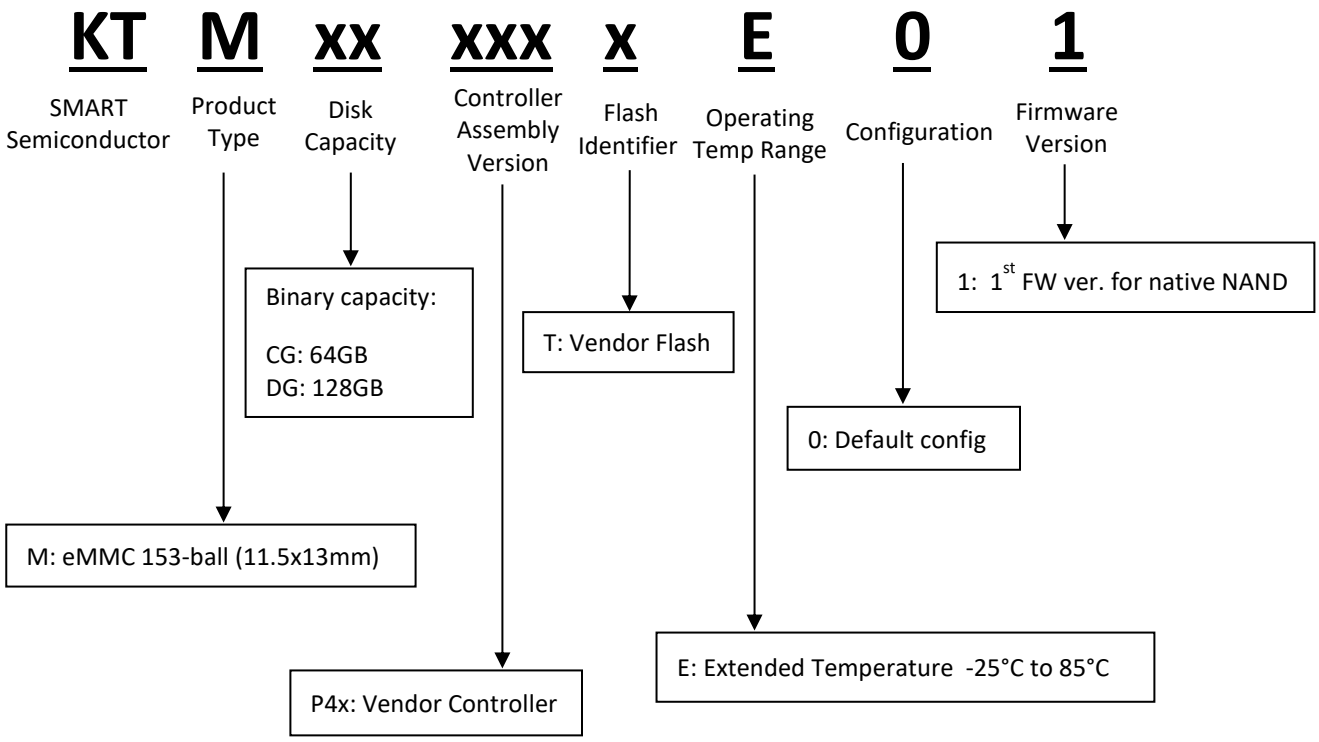
(1) Note: FIRMWARE_VERSION depends on capacity.

8 PART NUMBERS

Table 14: Part Numbering Information

Capacity	Part Number
64GB	KTMCGP4ATE01
128GB	KTMDGP4ATE01

8.1 Part Number Decoder



Note:

[1] Actual Firmware Revision as reported in ECSD [257:254] in ASCII

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