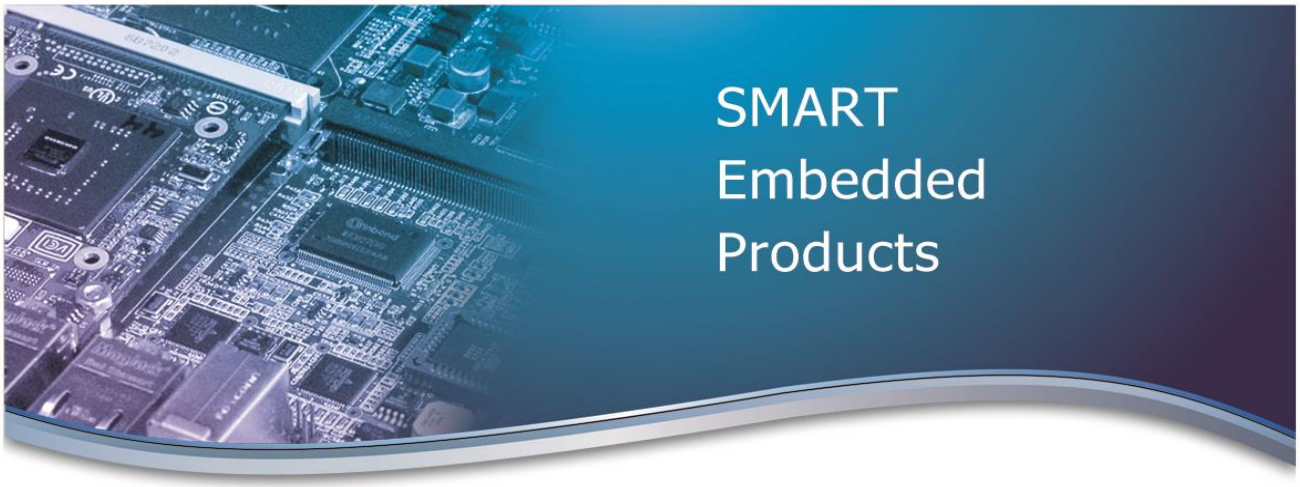


Product Specification

SMART MODULAR
BGAE340 eMMC Product Family
eMMC v5.1 100-ball BGA

SPQ8GH2AHIx1

March 2025
DSEM745-AE

www.smartm.com

REVISION HISTORY

Date	Revision	Section(s)	Description
January 2023	AA	All	Initial Release
June 2023	AB	Recommended Reflow Profiles	Updated Recommended Values
July 2023	AC	Page Cover	Updated Product Family Naming
January 2025	AD	All	Removed VCCQ 3.3V support
March 2025	AE	Part Number Information	Removed Wide Temperature

ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

SMART Modular Technologies, Inc.
39870 Eureka Dr.
Newark, CA 94560
(510) 623-1231 voice
(510) 623-1434 fax
info@smartm.com
An ISO 9001 certified company.

Features

- **Capacity**
  - 4GB (pSLC)
  - 8GB (Native MLC)
- **Electrical/Physical Interface**
  - Compliant with eMMC Specification Version 5.1
  - 100 Ball Standard BGA Packages
- **Bus Mode**
  - High-speed eMMC protocol
    - SDR52, DDR52, HS200, and HS400
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1-bit command, 8-bit data bus) and a hardware reset
- **Bus Width**
  - 1-bit, 4-bit, 8-bit
- **Performance (HS400)**
  - Read:
    - Up to 250MB/s
  - Write:
    - Up to 65MB/s
- **Operating Temperature[1]**
  - Industrial: -40°C to +85°C
- **Storage Temperature[2]**
  - -40°C to +85°C
- **Input Power:**
  - V_{CC}: 2.7 – 3.6V
  - V_{CCQ}: 1.7 – 1.95V
- **Power Consumption (HS400, I_{CC}/I_{CCQ})**
  - Read: 111/149mA
  - Write: 59/84mA
  - Standby: 110/470µA
- **Certification & Compliance**
  - RoHS
  - REACH
  - Green Package
- **NAND Technology**
  - MLC
- **Reliability**
  - Configurable error correction code (ECC)
  - Defect block management
  - Wear leveling
  - Garbage collection
  - Uncorrectable bit error rate (UBER): 1 sector per 10^{15} bits read
- **Security**
  - Sanitize, Discard, trim, Erase
  - Lock/Unlock, Secure Removal Type
  - Write protect, Secure Write Protection
- **Additional Features**
  - Field firmware update (FFU)
  - Production state awareness (PSA)
  - Device health report
  - Replay Protected Memory Block (RPMB)
  - Boot and Alternative Boot Mode
  - High Priority Interrupt (HPI)
  - Command Queuing
  - Configurable Drive Strength
  - Hardware/Software Reset
  - Cache flushing report
  - Cache barrier
  - PON, Sleep/Awake

NOTES:
[1] Ambient temperature.

General Description

Overview

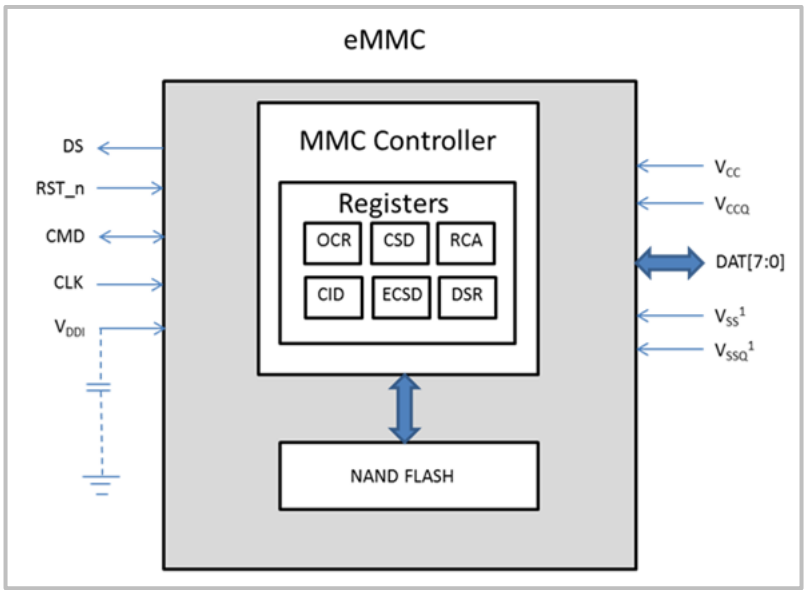
SMART Modular's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMART's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMART's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

Functional Block Diagram

eMMC Block Diagram



Performance

Performance Characteristics (MLC Partition Burst Performance)

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB (native) No pre-configuration	250	65	10000	2000

Capacity	H200 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB (native) No pre-configuration	180	65	9800	2000

Capacity	DDR52 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB (native) No pre-configuration	95	65	8000	2200

Performance measured based on the following conditions:
[1] Testmetrix VTESA-4100E; bus in x8 I/O mode. Write cache off.

Performance Characteristics (pSLC Partition Burst Performance)

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
4 GB (pSLC) Pre-configuration	250	65	10000	2000

Capacity	H200 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
4GB (pSLC) Pre-configuration	180	65	9800	2000

Capacity	DDR52 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
4GB (pSLC) Pre-configuration	95	65	8000	2200

Performance measured based on the following conditions:
[1] Testmetrix VTESA-4100E; bus in x8 I/O mode.

Endurance

Drive Lifetime[1]

Capacity	Value (Max)
8GB(Native)	20 TBW
4GB(pSLC)	100 TBW

[1] Endurance is related directly to the User Specific Workload. Measured with 100% Sequential Workload.

Reliability

Uncorrectable Bit Error Rate (UBER)

Failure Rate	8GB (Native)
FIT @ Tc = 55°C	62.17

Uncorrectable Bit Error Rate (UBER)

Parameter	Value
Data Reliability	< $1E^{-15}$ uncorrectable bit error rate

Data Retention

Parameter	Value
Data Retention (@ 40°C)	10 years when 90% life remaining
	1 year when 10% life remaining

Operating and Storage Temperature[1]

Parameter	Value	
Operating Temperature	Industrial	-40°C to +85°C
Storage Temperature	-40°C to +85°C	

[1] Operating temperature herein is Ambient Temperature.

Power (Current) Consumption

Condition[1]		I_{CC}/I_{CCQ} (Typical) 8GB (native)	Units
Write	DDR52	47/80	mA
	HS200	59/84	mA
	HS400	59/84	mA
Read	DDR52	42/149	mA
	HS200	80/149	mA
	HS400	111/149	mA
Idle		110/470	µA

[1] Bus in x8 I/O mode; 25°C. Measurements done as maximum RMS current consumption over 100 milliseconds.

Condition[1]		I_{CC}/I_{CCQ} (Typical) 4GB (pSLC)	Units
Write	DDR52	40/78	mA
	HS200	59/78	mA
	HS400	59/83	mA
Read	DDR52	45/145	mA
	HS200	86/145	mA
	HS400	109/145	mA
Idle		110/470	µA

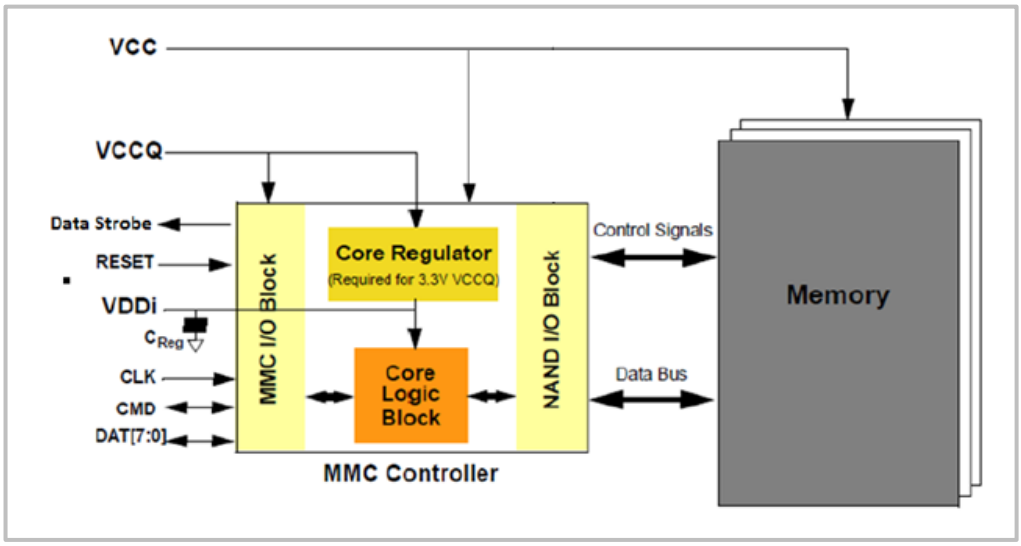
[1] Bus in x8 I/O mode; 25°C. Measurements done as maximum RMS current consumption over 100 milliseconds.

Electrical Specification

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is the supply voltage for controller and Flash memory power; V_{CCQ} is the supply voltage for controller and eMMC I/O voltage.

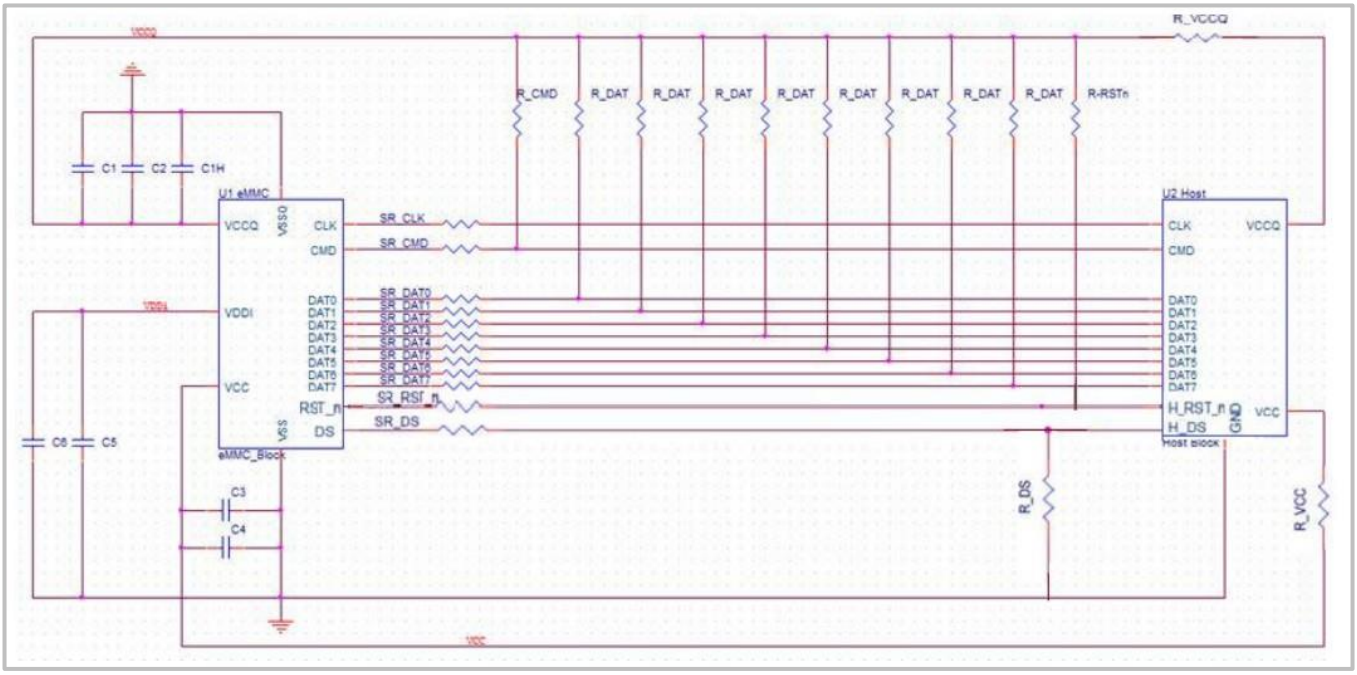
Power Connections



Power Requirements

Symbol	Parameter	Value (Minimum)	Value (Typical)	Value (Maximum)	Unit
V_{CC}	Voltage supply to Flash memory	2.7	3.3	3.6	V
V_{CCQ}	Voltage supply to host interface	1.70	1.80	1.95	V
V_{DDi}	Internal voltage regulator connection to external capacitor	-	-	-	-

Recommended eMMC Connection



Capacitor and Resistor Specifications

Parameter[1]	Symbol	Min.	Max.	Recom-mended	Unit	Remark
Pull-up resistance for CMD	R_CMD	4.7	50	10	kΩ	To prevent bus from floating
Pull-up resistance for DAT0-7	R_DAT	10	50	50	kΩ	To prevent bus from floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	50	kΩ	It's not necessary to put pull-up resistance on RST_n (H/W reset) line if host does not use H/W reset.
Pull-down resistance for DS	R_DS	10	50	50	kΩ	
Impedance on CLK/CMD/DAT0~7	-	45	55	50	Ω	Impedance match
Serial resistance on CLK	SR_CLK	-	-	22	Ω	To put serial resistance except 0 ohm, check timing are all in Spec.
Serial resistance on power trace	R_VCC R_VCCQ	-	-	0	Ω	Typical size 0603 or 0805.
Serial resistance on CMD/DS/DAT0~7/ RST_n	SR_CMD SR_DS SR_DAT0~7 SR_RST_n	-	-	0	Ω	To put serial resistance except 0 ohm, check timing are all in Spec.

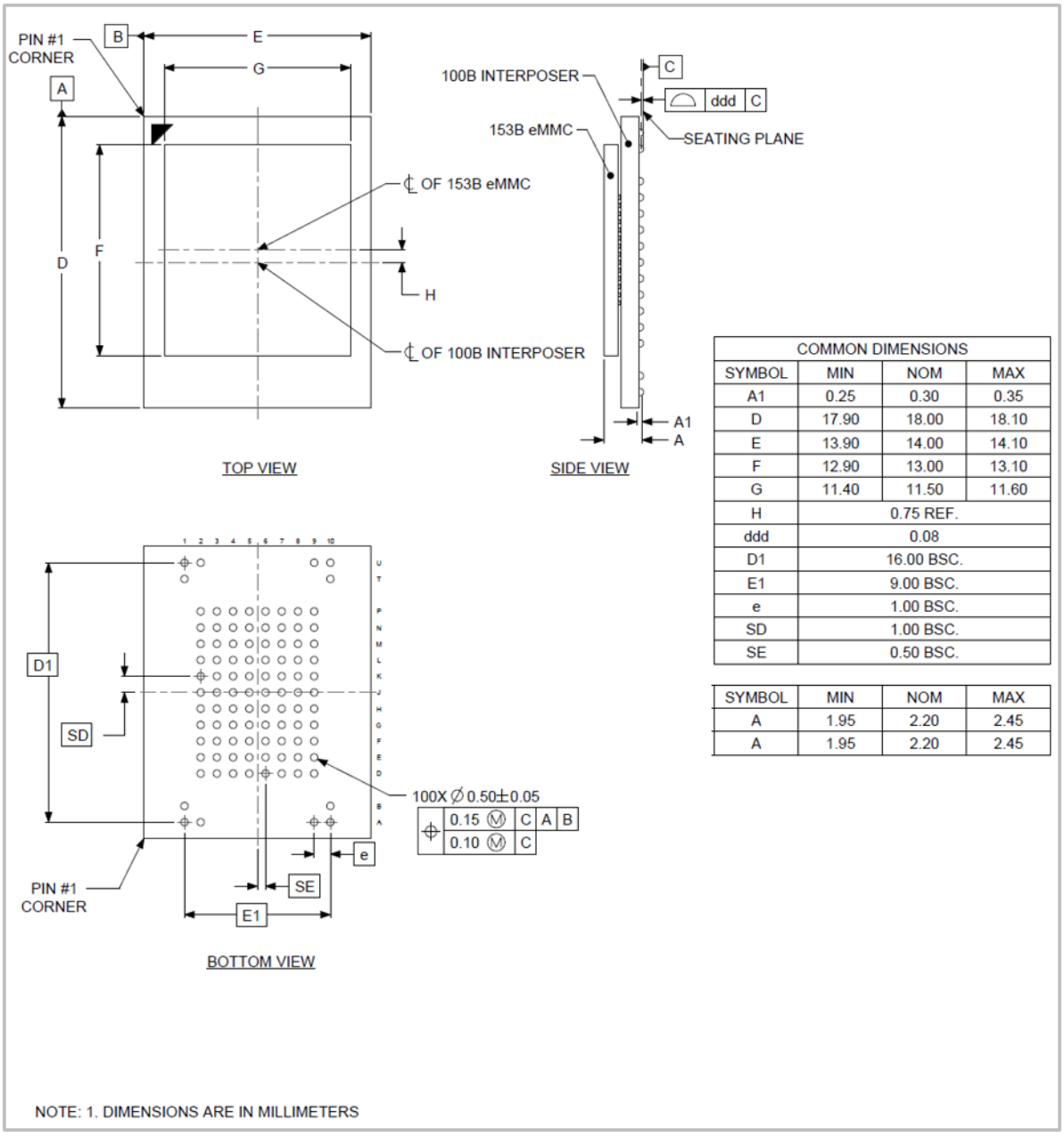
Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.
- Recommended Value and Quantity:
  VCCQ (C1,C2, C_{H1}): More than 0.1 µF x 1, 2.2 µF x 1, and 1 x 1 µF
  VCC (C3,C4): More than 0.1 µF x 1 and 2.2 µF x 1
  VDDi(C5,C6): More than 0.1 µF x 1 and 2.2 µF x 1
  A minimum of 1uF is required for VCCQ, VCC, and VDDi.

Customer requested to place all of the caps shown above. For VCCQ caps, they should be located as close as possible to the VCCQ/VSSQ balls near the DAT0-7 signals.

Mechanical Specification

100-Ball BGA Dimensions - 14 mm x 18 mm



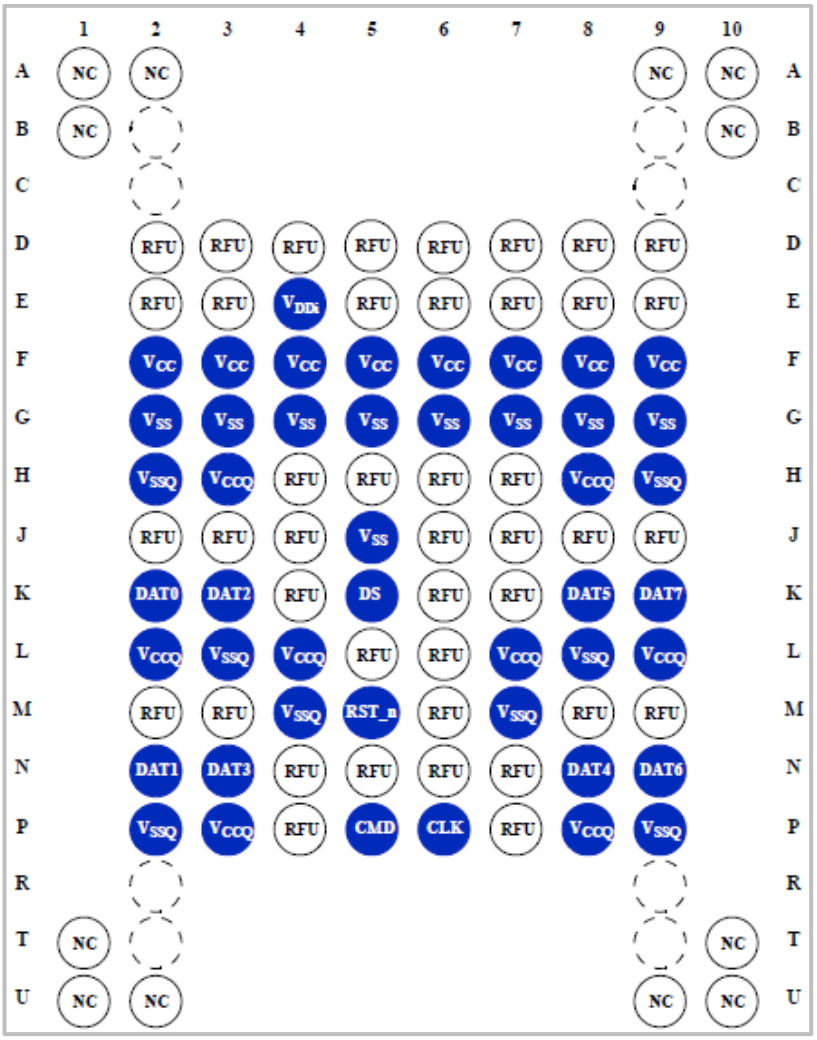
COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A1	0.25	0.30	0.35
D	17.90	18.00	18.10
E	13.90	14.00	14.10
F	12.90	13.00	13.10
G	11.40	11.50	11.60
H	0.75 REF.		
ddd	0.08		
D1	16.00 BSC.		
E1	9.00 BSC.		
e	1.00 BSC.		
SD	1.00 BSC.		
SE	0.50 BSC.		

SYMBOL	MIN	NOM	MAX
A	1.95	2.20	2.45
A	1.95	2.20	2.45

Mechanical Dimensions

Parameter	Value
Length	14.00 mm [0.55in]
Width	18.00 mm [0.71in]

100-Ball eMMC Ball-out Diagram (Top View, Ball Down)



Pinout Descriptions

Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock Signal.
RST_n	Input	Hardware Reset Signal.
CMD	I/O	Command Signal.
DAT[7:0]	I/O	Data Bus.
DS	Output	Data Strobe Signal, Used in HS400 mode.
V_{CC}	Supply	Supply voltage for controller and Flash memory power.
V_{CCQ}	Supply	Supply voltage for controller and eMMC I/O power.
V_{SS}	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
V_{SSQ}	Supply	Supply voltage ground for controller and IO Flash memory. Can be short with VSS.
V_{DDi}		Connect capacitor from VDDi to GND for stabilize internal power.
NC	-	In eMMC chip is no connect. Left it floating.
RFU	-	Reserved for future use. Left it floating for future use.

Recommended Reflow Profiles

Reflow Parameters	Suggested Range
Peak Temperature	235 - 245°C
Time Above Liquidus	45 - 70 seconds
Cooling Rate	< 4°C/s

Note: Each solder paste manufacturer will have their own reflow profile specification. The recommendation is to follow the solder paste manufacturer's reflow profile specification and optimize the reflow profile based on product complexity for the assembly process.

Registers

Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

CID Register Field Parameters

Name	Field	Width (Bits)	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	0x01
Reserved	-	6	[119:114]	--
Device / BGA	CBX	2	[113:112]	0x01
OEM/application ID	OID	8	[111:104]	0x00
Product name	PNM	48	[103:56]	0x533430303038
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN	32	[47:16]	--(1)
Manufacturing date	MDT	8	[15:8]	--(2)
CRC7 checksum	CRC	7	[7:1]	--(3)
reserved	-	1	0	--

1 The product name uses ASCII code and 'Δ' is a space (0x20).
2 Unique for each device. 32-bit unsigned binary integer.
3 2 hex digits for device manufacturing month and year.
4 CRC for CID register. Different for each device.

OCR Register Field Definitions

V_{DD} voltage window	Width (Bits)	OCR bits	OCR Value
Ready/Busy	1	[31]	card power up status bit (busy)[1]
Access Mode	2	[30:29]	10b
Reserved	5	[28:24]	--
VCCQ: 2.7-3.6V	9	[23:15]	1 1111 1111b
VCCQ: 2.0-2.6V	7	[14:8]	000 0000b
VCCQ: 1.70-1.95V	1	[7]	1b
Reserved	7	[6:0]	--

1 This bit is set to LOW if the device has not finished the power up routine.

2 The voltage for internal flash memory (VCC) should be 2.7-3.6V regardless of OCR Register value.

3 8GB Part number does not support VCCQ in 2.7-3.6V.

CSD Register Field Parameters

Name	Field	Width (Bits)	Cell Type[1]	CSD Bits	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	27h
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	1h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W	[9:8]	0h
CRC	CRC	7	R/W	[7:1]	-
Reserved(Not used, always'1')	-	1	-	[0:0]	-

1 R = Read-only
R/W = One-time programmable and readable

ECSD Register Field Parameters

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Reserved	--		6	--	[511:506]	--
Extended Security Commands Error	EXT_SECURITY_ERR		1	R	[505]	0x00
Supported command sets	S_CMD_SET		1	R	[504]	0x01
HPI features	HPI_FEATURES		1	R	[503]	0x01
Background operations support	BKOPS_SUPPORT		1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	8GB(Native) 4GB(pSLC)	1	R	[501]	0x20
Max packed write commands	MAX_PACKED_WRITES	8GB(Native) 4GB(pSLC)	1	R	[500]	0x20
Data tag support	DATA_TAG_SUPPORT		1	R	[499]	0x01
Tag unit size	TAG_UNIT_SIZE		1	R	[498]	0x00
Tag resources size	TAG_RES_SIZE		1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES		1	R	[496]	0x78
Large unit size	LARGE_UNIT_SIZE_M1		1	R	[495]	0x01
Extended partitions attribute support	EXT_SUPPORT		1	R	[494]	0x03
Supported Modes	SUPPORTED_MODES		1	R	[493]	0x01
FFU features	FFU_FEATURES		1	R	[492]	0x00
Operations code timeout	OPERATION_CODE_TIMEOUT		1	R	[491]	0x17
FFU Argument	FFU_ARG		4	R	[490:487]	0xFFFAFFF0
Reserved	--		181	--	[486:309]	--
CMD Queuing Support	CMDQ_ SUPPOR		1	R	[308]	0x01
CMD Queuing Depth	CMDQ_ DEPTH		1	R	[307]	0x1F
Reserved	--		1	--	[306]	--
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED		4	R	[305:302]	0x00
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT		32	R	[301:270]	0x00
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B		1	R	[269]	Variable

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A		1	R	[268]	Variable
Pre EOL information	PRE_EOL_INFO		1	R	[267]	Variable
Optimal read size	OPTIMAL_READ_SIZE		1	R	[266]	0x40
Optimal write size	OPTIMAL_WRITE_SIZE		1	R	[265]	0x40
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE		1	R	[264]	0x07
Device Version	Device version	8GB(Native) 4GB(pSLC)	2	R	[263:262]	0x3805
Firmware version	FIRMWARE_VERSION		8	R	[261:254]	--(1)
Power class for200MHz，DDR at VCC=3.6V	PWR_CL_DDR_200_360		1	R	[253]	0x00
Cache size	CACHE_SIZE		4	R	[252:249]	0x400
Generic CMD6 timeout	GENERIC_CMD6_TIME		1	R	[248]	0x05
Power off notification (long) timeout	POWER_OFF_LONG_TIME		1	R	[247]	0x64
Background operations status	BKOPS_STATUS		1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM		4	R	[245:242]	0x00
First initialization time after partitioning	INI_TIMEOUT_AP		1	R	[241]	0x0A
Reserved	--		1	--	[240]	--
Power class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360		1	R	[239]	0x00
Power class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195		1	R	[238]	0x00
Power class for 200 MHz at 1.95V, VCC = 3.6V	PWR_CL_200_195		1	R	[237]	0x00
Power class for 200 MHz at 1.3V, VCC = 3.6V	PWR_CL_200_130		1	R	[236]	0x00
Minimum write performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52		1	R	[235]	0x00
Minimum read performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52		1	R	[234]	0x00
Reserved	--		1	--	[233]	--
TRIM multiplier	TRIM_MULT		1	R	[232]	0x02

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Secure feature support	SEC_FEATURE_SUPPORT		1	R	[231]	0x55
SECURE ERASE multiplier	SEC_ERASE_MULT	8GB(Native) 4GB(pSLC)	1	R	[230]	0x19
SECURE TRIM multiplier	SEC_TRIM_MULT	8GB(Native) 4GB(pSLC)	1	R	[229]	0x0A
Boot information	BOOT_INFO		1	R	[228]	0x07
Reserved	--		1	--	[227]	--
Boot partition size	BOOT_SIZE_MULT		1	R	[226]	0x20
Access size	ACC_SIZE		1	R	[225]	0x06
High-capacity erase unit size	HC_ERASE_GRP_SIZE		1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_ MULT		1	R	[223]	0x02
Reliable write-sector count	REL_WR_SEC_C		1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE		1	R	[221]	0x10
Sleep current (V_{CC})	S_C_VCC		1	R	[220]	0x07
Sleep current (V_{CCQ})	S_C_VCCQ		1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_AWARENES S_TIMEOUT		1	R	[218]	0x17
Sleep/awake timeout	S_A_TIMEOUT	8GB(Native) 4GB(pSLC)	1	R	[217]	0x12
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME		1	R	[216]	0x0C
Sector count	SEC-COUNT	8GB	4	R	[215:212]	0x00E90000
		4GB(pSLC)				0x00748000
Reserved	--		1	--	[211]	--
Minimum write performance for 8-bit at 52 MHz	MIN_PERF_W_8_52		1	R	[210]	0x00
Minimum read performance for 8-bit at 52 MHz	MIN_PERF_R_8_52		1	R	[209]	0x00
Minimum write performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_W_8_26_4_52		1	R	[208]	0x00
Minimum read performance for 8-bit at 26 MHz and 4-bit at 52 MHz	MIN_PERF_R_8_26_4_52		1	R	[207]	0x00

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Minimum write performance for 4-bit at 26 MHz	MIN_PERF_W_4_26		1	R	[206]	0x00
Minimum read performance for 4-bit at 26 MHz	MIN_PERF_R_4_26		1	R	[205]	0x00
Reserved	--		1	--	[204]	--
Power class for 26 MHz at 3.6V 1 R	PWR_CL_26_360		1	R	[203]	0x00
Power class for 52 MHz at 3.6V 1 R	PWR_CL_52_360		1	R	[202]	0x00
Power class for 26 MHz at 1.95V 1 R	PWR_CL_26_195		1	R	[201]	0x00
Power class for 52 MHz at 1.95V 1 R	PWR_CL_52_195		1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	8GB(Native) 4GB(pSLC)	1	R	[199]	0x04
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	8GB(Native) 4GB(pSLC)	1	R	[198]	0x0A
I/O driver strength	DRIVER_STRENGTH		1	R	[197]	0x1F
Card type	CARD_TYPE		1	R	[196]	0x57
Reserved	--		1	--	[195]	--
CSD structure version	CSD_STRUCTURE		1	R	[194]	0x02
Reserved	--		1	--	[193]	--
Extended CSD revision	EXT_CSD_REV		1	--	[192]	0x08
Command set	CMD_SET		1	R/W/E_P	[191]	0x00
Reserved	--		1	--	[190]	--
Command set revision	CMD_SET_REV		1	R	[189]	0x00
Reserved	--		1	--	[188]	--
Power class	POWER_CLASS		1	R/W/E_P	[187]	0x00
Reserved	--		1	--	[186]	--
High-speed interface timing	HS_TIMING		1	R/W/E_P	[185]	0x00
Reserved	--		1	--	[184]	--
Bus width mode	BUS_WIDTH		1	W/E_P	[183]	0x00
Reserved	--		1	--	[182]	--
Erased memory content	ERASED_MEM_CONT		1	R	[181]	0x00

Name	Field		Size (Bytes)	Cell Type[1]	ECSD Bytes	ECSD Values
Reserved	--		1	--	[180]	--
Partition configuration	PARTITION_CONFIG		1	R/W/E, R/W/E_P	[179]	0x00
Boot config protection	BOOT_CONFIG_PROT		1	R/W, R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS		1	R/W/E	[177]	0x00
Reserved	--		1	--	[176]	--
High-density erase group definition	ERASE_GROUP_DEF		1	R/W/E_P	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS		1	R	[174]	0x00
Boot area write protection register	BOOT_WP		1	R/W, R/W/C_P	[173]	0x00
Reserved	--		1	-	[172]	--
User write protection register	USER_WP		1	R/W, R/W/C_P, R/W/E_P	[171]	0x00
Reserved	--		1	--	[170]	--
Firmware configuration	FW_CONFIG		1	R/W	[169]	0x00
RPMB size	RPMB_SIZE_MULT		1	R	[168]	0x20
Write reliability setting register	WR_REL_SET		1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM		1	R	[166]	0x15
Start sanitize operation	SANITIZE_START		1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START		1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	8GB(Native) 4GB(pSLC)	1	R/W	[163]	0x02
Hardware reset function	RST_n_FUNCTION		1	R/W	[162]	0x00
HPI management	HPI_MGMT		1	R/W/E/P	[161]	0x00
Partitioning support	PARTITIONING_SUPPORT		1	R/W/E, R/W/E_P	[160]	0x07
Maximum enhanced area size	MAX_ENH_SIZE_MULT	8GB(Native) 4GB(pSLC)	3	R	[159:157]	0x0001D2
Partitions attribute		8GB(Native)	1	R/W	[156]	0x00

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
	PARTITIONS_ATTRIBUTE	4GB(pSLC)				0x01
Partitioning setting	PARTITIONING_SETTING-COMPLETED	8GB(Native)	1	R/W	[155]	0x00
		4GB(pSLC)				0x01
General-purpose partition size	GP_SIZE_MULT		12	R/W	[154:143]	0x00
Enhanced user data area size	ENH_SIZE_MULT	8GB(Native)	3	R/W	[142:140]	0x00
		4GB(pSLC)				0x1D2
Enhanced user data start address	ENH_START_ADDR		4	R/W	[139:136]	0x00
Reserved	-		1	-	[135]	--
Bad block management mode	SEC_BAD_BLK_MGMNT		1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS		1	R/W/E	[133]	0x00
Package case temperature is controlled	TCASE_SUPPORT		1	W/E_P	[132]	0x00
Periodic wake-up	PERIODIC_WAKEUP		1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	8GB(Native) 4GB(pSLC)	1	R	[130]	0x01
Reserved	-		2	-	[129:128]	--
Vendor specific fields	VENDOR_SPECIFIC_NFIELD		64	<vs>	[127:64]	0x00
Native sector size	NATIVE_SECTOR_SIZE		1	R	[63]	0x01
Sector size emulation	USE_NATIVE_SECTOR		1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE		1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU		1	R	[60]	0x0A
Class 6 command control	CLASS_6_CTRL		1	R/W/E_P	[59]	0x00
Number of addressed groups to be released	DYNCAP_NEEDED		1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS_CTRL		2	R/W/E_P	[57:56]	0x00
Exception events status	EXCEPTION_EVENTS_STATUS		2	R	[55:54]	0x00
Extended partitions attribute	EXT_PARTITIONS_ATTRIBUTE		2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF		15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND_STATUS		1	R	[36]	0x00

Name	Field		Size (Bytes)	Cell Type(1)	ECSD Bytes	ECSD Values
Packed command failure index	PACKED_FAILURE_INDEX		1	R	[35]	0x00
Power off notification	POWER_OFF_NOTIFICATION		1	R/W/E_P	[34]	0x00
Control to turn the cache on/off	CACHE_CTRL		1	R/W/E_P	[33]	0x00
Flushing of the cache	FLUSH_CACHE		1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL		1	R/W	[31]	0x00
Mode config	MODE_CONFIG		1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_CODES		1	W/E_P	[29]	0x00
Reserved	-		2	-	[28:27]	--
FFU status	FFU_STATUS		1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA_SIZE		4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING _DATASIZE	8GB(Native) 4GB(pSLC)	4	R	[21:18]	0x00E90000
Product state awareness enablement	PRODUCT_STATE_AWARENESS_E NABLEMENT		1	R/W/E & R	[17]	0x01
Secure removal type	SECURE_REMOVAL_TYPE		1	R/W & R	[16]	0x3B
Reserved	-		16	-	[15:0]	--

1 R = Read-only
R/W = One-time programmable and readable
R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not cleared by CMD0 reset) and readable
R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable
W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable
2 It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.
3 This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing (see Section 10.6.1 of JESD84-B50). If the host sets value 2 the Device changes its timing to HS200 interface timing (see Section 10.8.1 of JESD84-B50), If the host sets HS_TIMING[3:0] to 0x3,the device changes its timing to HS400 interface timing (see10.10 of JESD84-B50).
4 The purpose and type of these fields are reserved for definition by the device manufacturer.
5 These registers have different values in enhanced mode

Part Numbers

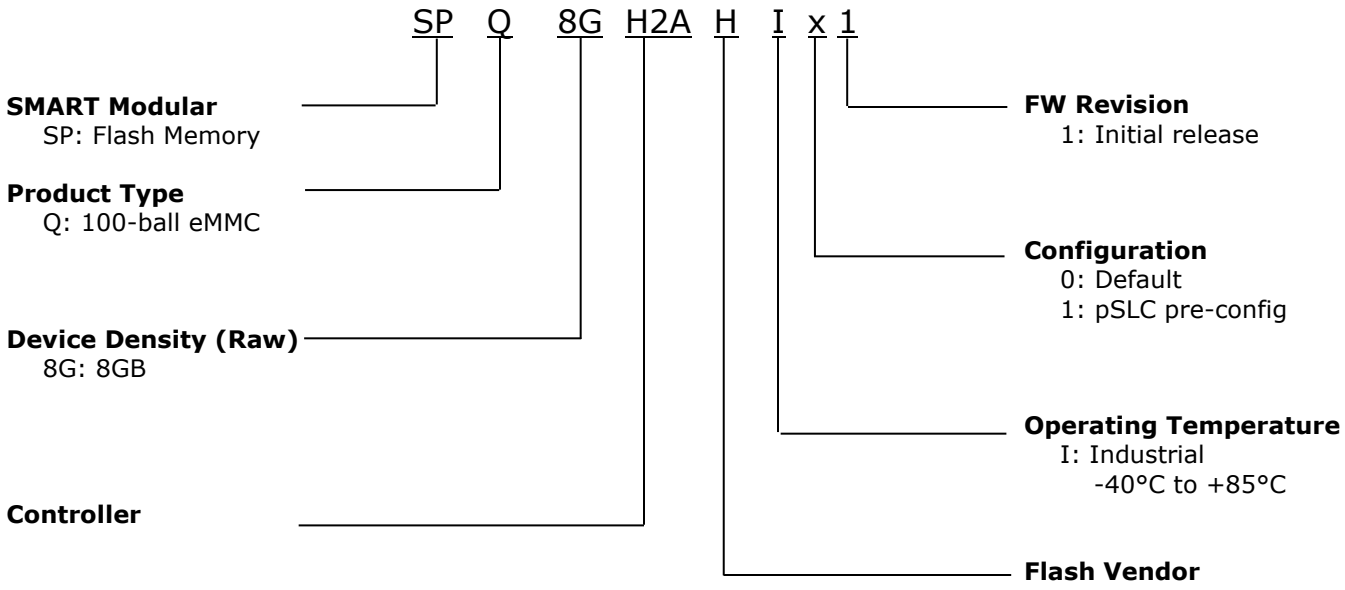
Part Numbering Information

The following table lists the available devices for this family.

Part Numbering Information

Part Number	Capacity
Native MLC	
SPQ8GH2AHI01	8GB
Pre-Configured to pSLC	
SPQ8GH2AHI11	4GB

Part Number Decoder



Declaration of Conformity

Responsible Party Name:	SMART Modular Technologies, Inc.
Address:	39870 Eureka Drive Newark, CA 94560-4809, USA
Phone:	+1-510-623-1231

Hereby declares that the products:

SPQ8GH2AHIx1

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU and its amendments

Restriction of the use of hazardous substances in electrical and electronic equipment

- **EN 50581:2012**
  Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: March 3, 2025 10:47 AM

Representative in the European Union (for regulatory topics only):
Mr. Dermot Kelly,
SMART Subcontract Manager
CTP Prague Airport, Na Staré silnici 185
252 68 Kněževes (Ramp 320), Czech Republic
Phone +420-739-242-669, email: Dermot.Kelly@smartm.com

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