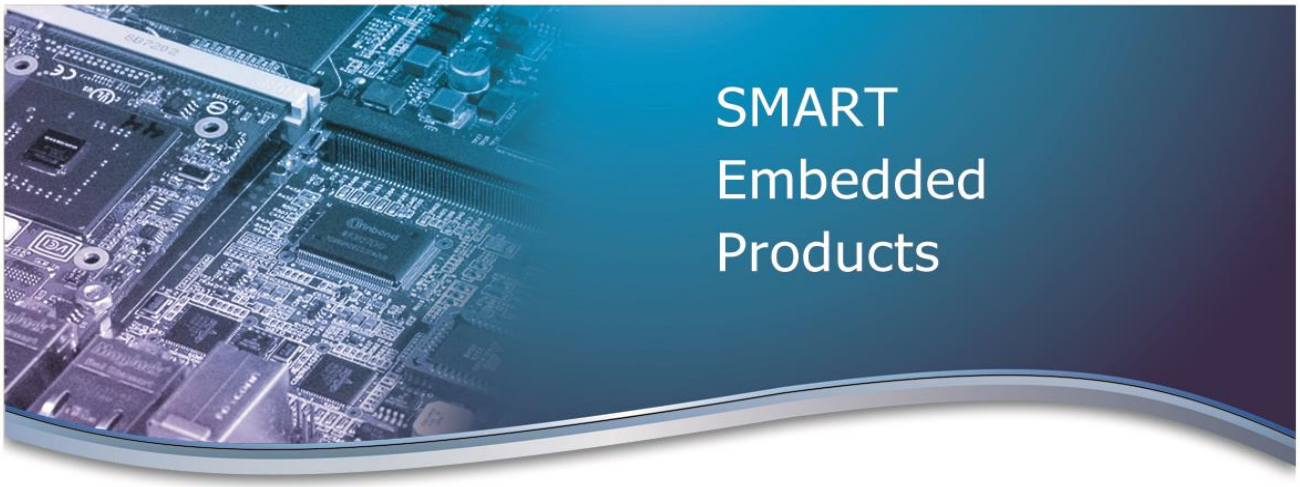

Product Specification

SMART MODULAR
BGAE340 eMMC Product Family
eMMC v5.1 100-ball BGA

SP9QxGH2AHW01

February 2025
DSEM968-AA

www.smartm.com

REVISION HISTORY

Date	Revision	Section(s)	Description
February 2025	AA	All	Initial Release

ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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An ISO 9001 certified company.

Features

- **Capacity**
  - 8GB and 16GB
- **Electrical/Physical Interface**
  - Compliant with eMMC Specification Version 5.1
  - 100 Ball Standard BGA Packages
- **Bus Mode**
  - High-speed eMMC protocol
    - SDR52, DDR52, HS200, and HS400
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1-bit command, 8-bit data bus) and a hardware reset
- **Bus Width**
  - 1-bit, 4-bit, 8-bit
- **Performance (HS400)**
  - Read:
    - Up to 275MB/s
  - Write:
    - Up to 94MB/s
- **Operating Temperature[2]**
  - Wide: -40°C to +105°C
- **Storage Temperature[2]**
  - -40°C to +105°C
- **Input Power:**
  - V_{CC}: 2.7 – 3.6V
  - V_{CCQ} : 1.7 – 1.95V
- **Power Consumption (HS400, I_{CC}/I_{CCQ})**
  - Read: 111/150mA
  - Write: 73/82mA
  - Standby: 220/870µA
- **Certification & Compliance**
  - RoHS
  - REACH
  - Green Package
- **NAND Technology**
  - MLC
- **Reliability**
  - Configurable error correction code (ECC)
  - Defect block management
  - Wear leveling
  - Garbage collection
  - Uncorrectable bit error rate (UBER): 1 sector per 10^{15} bits read
- **Security**
  - Sanitize, Discard, trim, Erase
  - Lock/Unlock, Secure Removal Type
  - Write protect, Secure Write Protection
- **Additional Features**
  - Field firmware update (FFU)
  - Production state awareness (PSA)
  - Device health report
  - Replay Protected Memory Block (RPMB)
  - Boot Feature and Boot Partition
  - High Priority Interrupt (HPI)
  - Command Queuing
  - Configurable Drive Strength
  - Hardware/Software Reset
  - Cache flushing report
  - Cache barrier
  - PON, Sleep/Awake

NOTES:

[1] HS200 and HS400 modes are supported only when V_{CCQ} is in 1.7 – 1.95V.

[2] Ambient temperature.

General Description

Overview

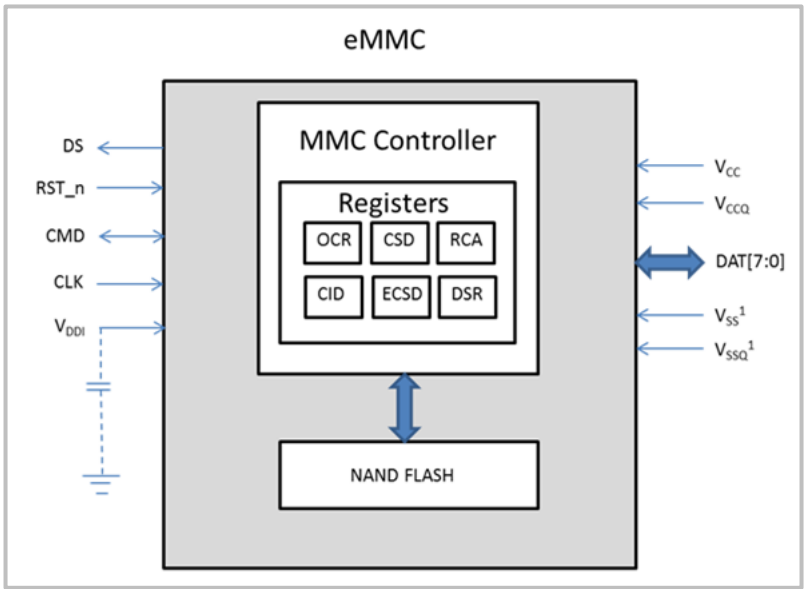
SMART Modular's eMMC Product Family is an embedded Flash storage solution in a small BGA package designed specifically for the most demanding applications. SMART's eMMC products address the need for enhanced reliability by incorporating on-board error detection and correction, wear leveling algorithms, and other data management techniques to provide reliable operation and maximum NAND media life expectancy over the product life cycle.

Additionally, the eMMC controller and firmware hide the increased complexities of NAND media from the host processor and allow for faster product development and time to market.

Target applications for SMART's eMMC solution include but are not limited to IoT, Set Top Box, Industrial and Networking appliances wanting a rugged yet cost effective high density mass storage solution.

Functional Block Diagram

eMMC Block Diagram



Performance

Performance Characteristics (MLC Partition Burst Performance)

Capacity	HS400 Performance			
	Seq. Read (MB/s)	Seq. Write (MB/s)	Random Read 4KB (IOPS)	Random Write 4KB (IOPS)
8GB	265	68	6290	1873
16GB	275	94	7290	1886

Performance measured based on the following conditions:
[1] Bus in x8 I/O, HS400 mode. Write cache off.

Endurance

Drive Lifetime[1]

Capacity	Value (Max)
8GB	20 TBW
16GB	40 TBW

[1] Endurance is related directly to the User Specific Workload. Measured with 100% Sequential Workload.

Reliability

Uncorrectable Bit Error Rate (UBER)

Failure Rate	8GB	16GB
FIT @ Tc = 72°C	39.88	59.95

Uncorrectable Bit Error Rate (UBER)

Parameter	Value
Data Reliability	< $1E^{-15}$ uncorrectable bit error rate

Data Retention

Parameter	Value
Data Retention (@ 55°C)	10 years when 90% life remaining
	1 year when 10% life remaining

Operating and Storage Temperature[1]

Parameter	Value	
Operating Temperature	Wide	-40°C to +105°C
Storage Temperature	-40°C to +105°C	

[1] Operating temperature herein is Ambient Temperature.

Power (Current) Consumption

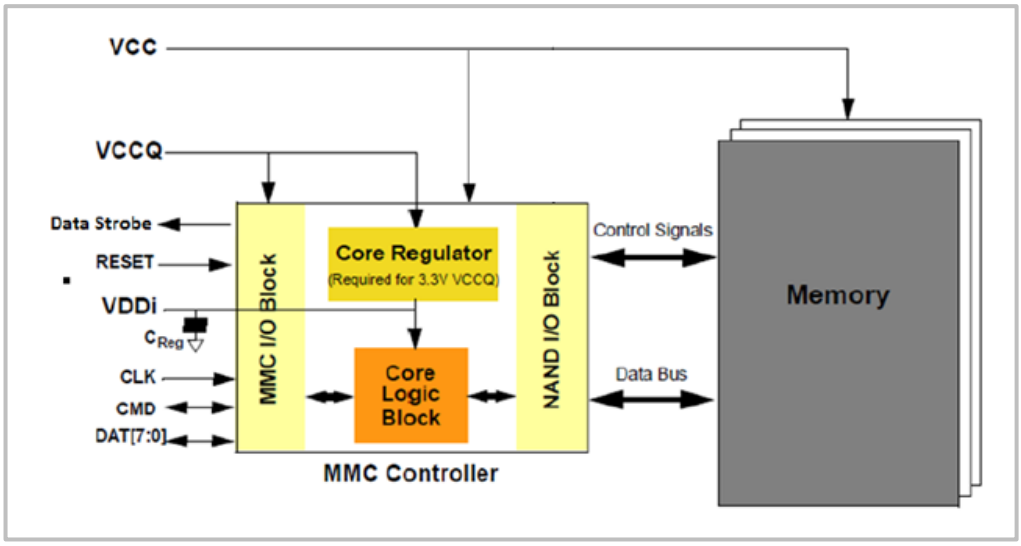
Condition		I_{CC}/I_{CCQ} (Typical)		Units
		8GB	16GB	
Write	DDR52	45/74	43/65	mA
	HS200	59/84	62/78	mA
	HS400	59/82	73/79	mA
Read	DDR52	42/123	34/109	mA
	HS200	80/121	65/119	mA
	HS400	111/144	99/150	mA
Idle		110/470	220/870	uA

Electrical Specification

The device current consumption for various device configurations is defined in the power class fields of the ECSD register.

V_{CC} is the supply voltage for controller and Flash memory power; V_{CCQ} is the supply voltage for controller and eMMC I/O voltage.

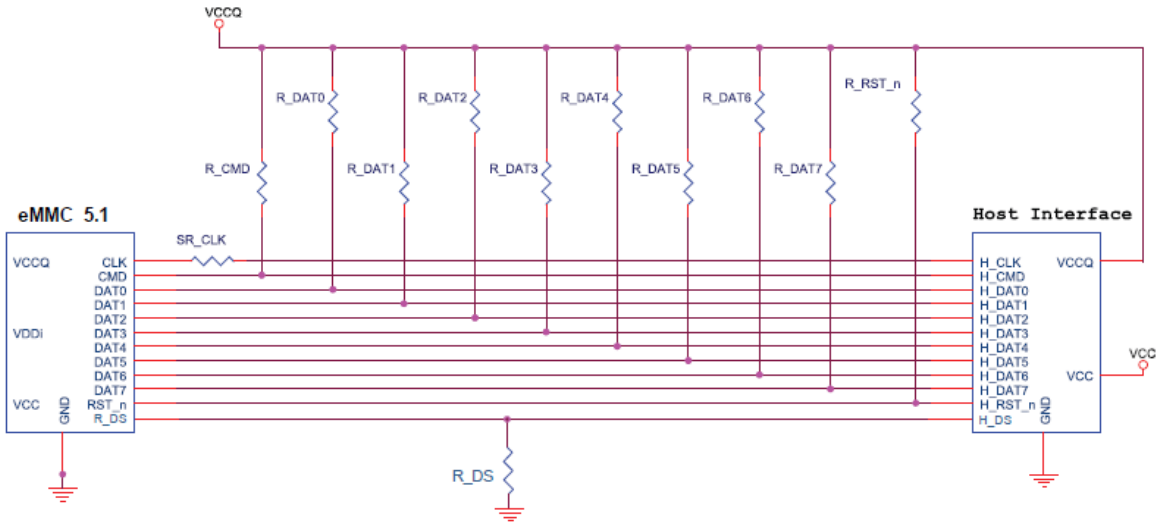
Power Connections



Power Requirements

Symbol	Parameter	Value (Minimum)	Value (Typical)	Value (Maximum)	Unit
V_{CC}	Voltage supply to Flash memory	2.7	3.3	3.6	V
V_{CCQ}	Voltage supply to host interface	1.70	1.80	1.95	V
V_{DDi}	Internal voltage regulator connection to external capacitor	-	-	-	-

Recommended eMMC Connection



Parameter	Symbol	Recommended	Comments
Pull-up resistance for CMD	R_CMD	10 kΩ	To prevent bus floating.
Pull-up resistance for DAT[7:0]	R_DAT	50 kΩ	To prevent bus floating.
Pull-up resistance for RST_n	R_RST_n	50 kΩ	A pull-up resistance on the RST_n (H/W reset) line is not required if the host does not enable the H/W reset feature.
Series termination for CLK	SR_CLK	22Ω	To stabilize the clock signal. It is recommend for customers to perform simulations using the controller IBIS model to confirm this value.
Pull-Down resistance for Data Strobe	R_DS	50 kΩ	

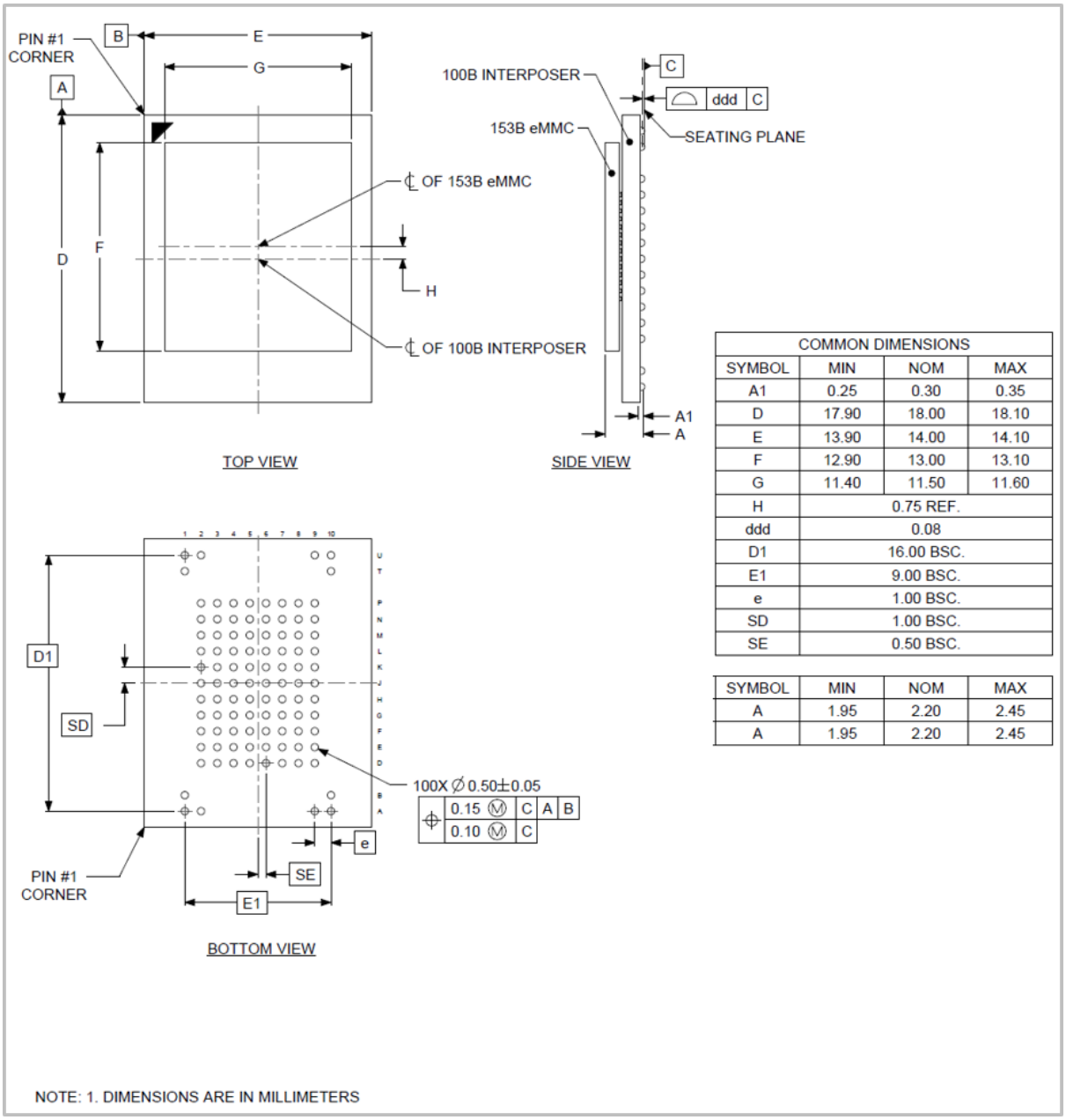
Decoupling Capacitor Recommendations

- X7R or X5R capacitors are recommended with a rated voltage > 6.3V.
- 0603 or a smaller size is recommended.
- Pick capacitors with low ESL and ESR.
- It is important to place decoupling caps as close to the target supply balls while maintaining > 20 mil trace width for supply connections to capacitor SMT pads.
- Recommended Value and Quantity:
  VCCQ: More than 0.1 µF x 1, 2.2 µF x 1, and 1 x 1 µF
  VCC: More than 0.1 µF x 1 and 2.2 µF x 1
  VDDi: More than 0.1 µF x 1 and 2.2 µF x 1
  A minimum of 1uF is required for VCCQ, VCC, and VDDi.

Customer is requested to place all of the caps shown above. For VCCQ caps, they should be located as close as possible to the VCCQ/VSSQ balls near the DAT0-7 signals.

Mechanical Specification

100-Ball BGA Dimensions - 14 mm x 18 mm



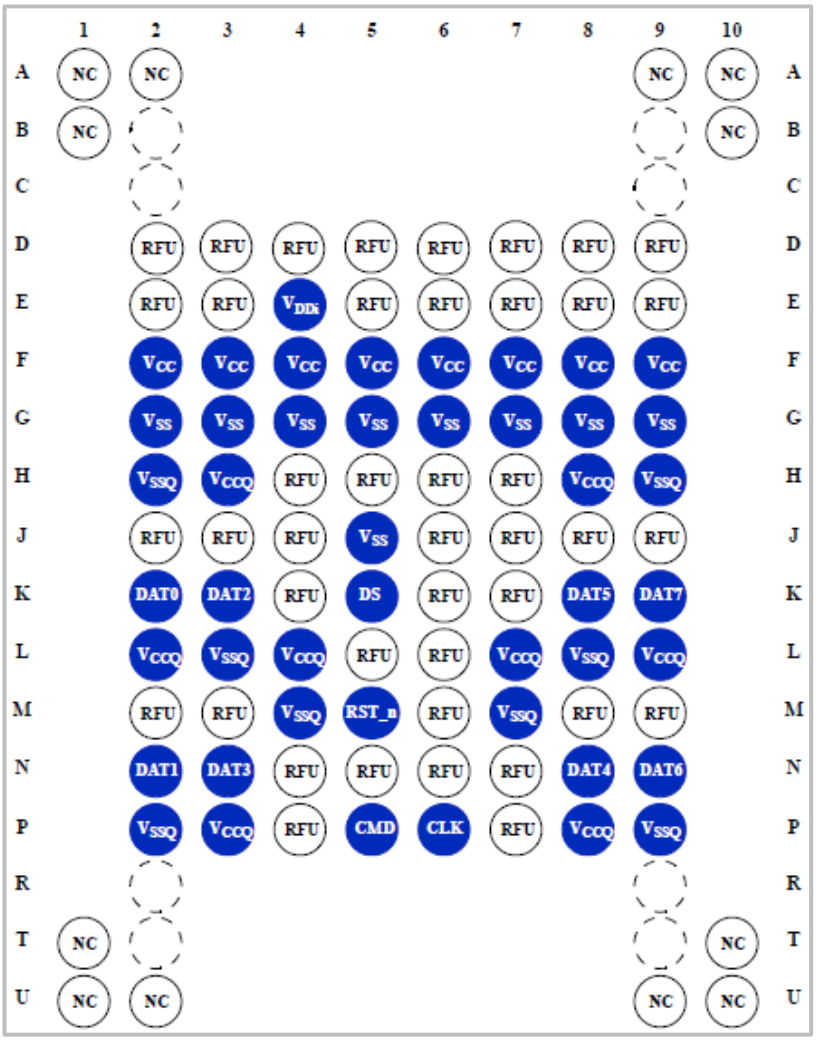
COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A1	0.25	0.30	0.35
D	17.90	18.00	18.10
E	13.90	14.00	14.10
F	12.90	13.00	13.10
G	11.40	11.50	11.60
H	0.75 REF.		
ddd	0.08		
D1	16.00 BSC.		
E1	9.00 BSC.		
e	1.00 BSC.		
SD	1.00 BSC.		
SE	0.50 BSC.		

SYMBOL	MIN	NOM	MAX
A	1.95	2.20	2.45
A	1.95	2.20	2.45

Mechanical Dimensions

Parameter	Value
Length	14.00 mm [0.55in]
Width	18.00 mm [0.71in]

100-Ball eMMC Ball-out Diagram (Top View, Ball Down)



Pinout Descriptions

Signal Descriptions

Symbol	Type	Description
CLK	Input	Clock Signal.
RST_n	Input	Hardware Reset Signal.
CMD	I/O	Command Signal.
DAT[7:0]	I/O	Data Bus.
DS	Output	Data Strobe Signal, Used in HS400 mode.
V_{CC}	Supply	Supply voltage for controller and Flash memory power.
V_{CCQ}	Supply	Supply voltage for controller and eMMC I/O power.
V_{SS}	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ.
V_{SSQ}	Supply	Supply voltage ground for controller and IO Flash memory. Can be short with VSS.
V_{DDi}		Connect capacitor from VDDi to GND for stabilize internal power.
NC	-	In eMMC chip is no connect. Left it floating.
RFU	-	Reserved for future use. Left it floating for future use.

Recommended Reflow Profiles

Reflow Parameters	Suggested Range
Peak Temperature	235 - 245°C
Time Above Liquidus	45 - 70 seconds
Cooling Rate	< 4°C/s

Note: Each solder paste manufacturer will have their own reflow profile specification. The recommendation is to follow the solder paste manufacturer's reflow profile specification and optimize the reflow profile based on product complexity for the assembly process.

Registers

Supported Device Registers

Name	Width	Description
CID	128 (Bits)	Card Identification
OCR	32 (Bits)	Operation Condition Register
CSD	128 (Bits)	Card Specific Data
ECSD	512 (Bytes)	Extended Card Specific Data

CID Register Field Parameters

Name	Field	Width (Bits)	CID Bits	CID Value
Manufacturer ID	MID	8	[127:120]	01h
Card BGA	CBX	2	[113:112]	01b
OEM/Application ID	OID	8	[111:104]	00h
Product Name	PNM	48	[103:56]	See product table
Product Revision	PRV	8	[55:48]	(Note3)
Product Serial Number	PSN	32	[47:16]	32-bit unsigned binary integer assigned at random
Manufacturing Date	MDT	8	[15:8]	(Note 1)
CRC7 Checksum	CRC	7	[7:1]	(Note 2)
Not Used	—	1	[0]	Always 1

1 Descriptions follow JEDEC e.MMC Standard Specifications.
2 The CRC7 checksum (7 bits). This is the checksum of the CID contents computed according to 0.
3 Product Revision is a combination of Controller and Firmware Revisions.

OCR Register Field Definitions

V_{DD} voltage window	OCR bits	OCR Value
Reserved	[6:0]	00 00000b
V_{CCQ}: 1.7 - 1.95 range	[7]	Dual Voltage: 1b
V_{CCQ}: 2.0 - 2.6 range	[14:8]	000 0000b
V_{CCQ}: 2.7 - 3.6 range	[23:15]	1 1111 1111b
Reserved	[28:24]	0 0000b
Access Mode	[30:29]	Sector Mode: 10b
e.MMC power up status bit (busy) (1)	[31]	—

1 This bit is set to LOW if the device has not finished the power up routine.

CSD Register Field Parameters

Field Name	Field ID	Size (Bits)	Cell Type	CSD Slice	CSD Value
CSD Structure	CSD_STRUCTURE	2	R	[127:126]	3h
System Specification Version	SPEC_VERS	4	R	[125:122]	4h
Reserved[1]	—	2	R	[121:120]	—
Data Read Access Time 1	TAAC	8	R	[119:112]	27h
Data Read Access Time 2 in CLK	NSAC	8	R	[111:104]	01h
Maximum Bus Clock Frequency	TRAN_SPEED	8	R	[103:96]	32h
Device Command Classes	CCC	12	R	[95:84]	0F5h
Maximum Read Block Length	READ_BL_LEN	4	R	[83:80]	9h
Partial Blocks For Read Allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write Block Misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read Block Misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR Implemented	DSR_IMP	1	R	[76:76]	0h
Reserved[1]	—	2	R	[75:74]	—
Device Size	*C_SIZE	12	R	[73:62]	FFFh
Maximum Read Current at VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Maximum Read Current at VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Maximum Write Current at VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Maximum Write Current at VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device Size Multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase Group Size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase Group Size Multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write Protect Group Size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write Protect Group Enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer Default	DEFAULT_ECC	2	R	[30:29]	0h
Write Speed Factor	R2W_FACTOR	3	R	[28:26]	2h
Maximum Write Data Block Length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial Blocks For Write Allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved[1]	—	4	R	[20:17]	—
Content Protection Application	CONTENT_PROT_APP	1	R	[16:16]	0h
File Format Group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy Flag (OTP)	COPY	1	R/W	[14:14]	1h
Permanent Write Protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary Write Protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File Format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC Code	ECC	2	R/W/E	[9:8]	0h
Calculated CRC	CRC	7	R/W/E	[7:1]	Note4
Not Used	—	1	—	[0]	Always 1

1. Reserved bits should be read at '0'.
2. R = Read only. R/W = One time programmable and readable. R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
3. VDD represents the total consumed current for V_{CC} and V_{CCQ}.
4. The CRC field carries the check sum for the CSD contents. It is computed according to 0. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

ECSD Register Field Parameters

Field Name	Field ID	Size (Bytes)	Cell Type	EXT_CSD Slice	Value
Reserved[5]	—	6	—	[511:506]	—
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	00h
Supported Command Sets	S_CMD_SET	1	R	[504]	01h
HPI Features	HPI_FEATURES	1	R	[503]	01h
Background Operations Support	BKOPS_SUPPORT	1	R	[502]	01h
Max Packed Read Commands	MAX_PACKED_READS	1	R	[501]	20h
Max Packed Write Commands	MAX_PACKED_WRITES	1	R	[500]	20h
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	01h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	00h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	00h
Context Management Capabilities	CONTEXT_CAPABILITIES	1	R	[496]	78h
Large Unit Size	LARGE_UNIT_SIZE_M1	1	R	[495]	01h
Extended Partitions Attribute Support	EXT_SUPPORT	1	R	[494]	03h
Supported Modes	SUPPORTED_MODES	1	R	[493]	01h
FFU Features	FFU_FEATURES	1	R	[492]	00h
Operation Codes Timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	17h
FFU Argument	FFU_ARG	4	R	[490:487]	FFFAFFF0h
Barrier support	BARRIER_ SUPPORT	1	R	486	1h
Reserved[5]		181	—	[485:309]	—
CMD Queuing Support	CMDQ_ SUPPORT	1	R	308	0h
CMD Queuing Depth	CMDQ_ DEPTH	1	R	307	00h
Reserved[5]		1	—	306	—
Number of FW Sectors Correctly Programmed	NUMBER_OF_FW_SECTORS_ CORRECTLY_PROGRAMMED	4	R	[305:302]	0000h
Vendor proprietary health report[11]	VENDOR_PROPRIETARY_HEALTH_ REPORT	32	R	[301:270]	N/A
Device Life Time Estimation Type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	Variable
Device Life Time Estimation Type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	Variable
Pre-EOL Information [9]	PRE_EOL_INFO	1	R	[267]	Variable
Optimal Read Size	OPTIMAL_READ_SIZE	1	R	[266]	40h
Optimal Write Size	OPTIMAL_WRITE_SIZE	1	R	[265]	40h
Optimal Trim Unit Size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	07h
Device Version	DEVICE_VERSION	2	R	[263:262]	3805h (For 8GB) 4105h (For 16GB)
Firmware Version[10]	FIRMWARE_VERSION	8	R	[261:254]	—
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	00h
Cache Size	CACHE_SIZE	4	R	[252:249]	0400h
Generic CMD6 Timeout	GENERIC_CMD6_TIME	1	R	[248]	05h
Power Off Notification (Long) Timeout	POWER_OFF_LONG_TIME	1	R	[247]	64h

Background Operations Status	BKOPS_STATUS	1	R	[246]	00h
Number Of Correctly Programmed Sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0000h
1st Initialization Time after Partitioning	INI_TIMEOUT_PA	1	R	[241]	0Ah
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	01h
Power Class for 52 MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	00h
Power Class for 52 MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	00h
Power Class for 200 MHz at 1.95V	PWR_CL_200_195	1	R	[237]	00h
Power Class for 200 MHz at 1.30V	PWR_CL_200_130	1	R	[236]	00h
Minimum Write Performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	00h
Minimum Read Performance for 8-bit at 52 MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	00h
Reserved[5]	—	1	—	[233]	—
Trim Multiplier	TRIM_MULT	1	R	[232]	02h
Secure Feature Support	SEC_FEATURE_SUPPORT	1	R	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	19h
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0Ah
Boot Information	BOOT_INFO	1	R	[228]	07h
Reserved[5]	—	1	—	[227]	—
Boot Partition Size	BOOT_SIZE_MULTI	1	R	[226]	20h
Access Size	ACC_SIZE	1	R	[225]	06h
High Capacity Erase Unit Size	HC_ERASE_GRP_SIZE	1	R	[224]	01h
High Capacity Erase Time Out	ERASE_TIMEOUT_MULT	1	R	[223]	02h
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	01h
High Capacity Write Protect Group Size	HC_WP_GRP_SIZE	1	R	[221]	10h
Sleep Current [VCC]	S_C_VCC	1	R	[220]	07h
Sleep Current [VCCQ]	S_C_VCCQ	1	R	[219]	07h
Production State Awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h
Sleep/awake Time Out	S_A_TIMEOUT	1	R	[217]	12h
Sleep Notification Timeout	SLLEP_NOTIFICATION_TIME	1	R	[216]	0Ch
Sector Count	SEC_COUNT	4	R	[215:212]	00E90000h for 8GB 1D20000h for 16GB
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	01h
Minimum Write Performance for 8-bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0h
Minimum Read Performance for 8-bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0h
Minimum Write Performance for 4-bit at 52 MHz or 8-bit at 26 MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h
Minimum Read Performance for 4-bit at 52 MHz or 8-bit at 26 MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h
Minimum Write Performance for 4-bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0h
Minimum Read Performance for 4-bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0h
Reserved[5]	—	1	—	[204]	—

Power Class for 26 MHz at 3.6 V	PWR_CL_26_360	1	R	[203]	0h
Power Class for 52 MHz at 3.6V	PWR_CL_52_360	1	R	[202]	0h
Power Class for 26 MHz at 1.95V	PWR_CL_26_195	1	R	[201]	0h
Power Class for 52 MHz at 1.95V	PWR_CL_52_195	1	R	[200]	0h
Partition Switching Timing	PARTITION_SWITCH_TIME	1	R	[199]	04h
Out-of-Interrupt Busy Timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0Ah
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	1Fh
Device Type	CARD_TYPE	1	R	[196]	57h
Reserved[5]	—	1	—	[195]	—
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	2h
Reserved[5]	—	1	—	[193]	—
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	8h
Command Set	CMD_SET	1	R/W/E_P	[191]	0h
Reserved[5]	—	1	—	[190]	—
Command Set Revision	CMD_SET_REV	1	R	[189]	0h
Reserved[5]	—	1	—	[188]	—
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0h
Reserved[5]	—	1	—	[186]	—
High Speed Interface Timing[6]	HS_TIMING	1	R/W/E_P	[185]	0h
Strobe Support	STROBE_SUPPORT	1	R	[184]	1h
Bus Width Mode [7]	BUS_WIDTH	1	W/E_P	[183]	0h
Reserved[5]	—	1	—	[182]	—
Erased Memory Content	ERASED_MEM_CONT	1	R	[181]	0h
Reserved[5]	—	1	—	[180]	—
Partition Configuration	PARTITION_CONFIG	1	R/W/E, R/W/E_P	[179]	0h
Boot Config Protection	BOOT_CONFIG_PROT	1	R/W, R/W/C_P	[178]	0h
Boot Bus Conditions	BOOT_BUS_WIDTH	1	R/W/E	[177]	0h
Reserved[5]	—	1	—	[176]	—
High-Density Erase Group Definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0h
Boot Write Protection Status Register	BOOT_WP_STATUS	1	R	[174]	0h
Boot Area Write Protect Register	BOOT_WP	1	R/W, R/W/C_P	[173]	0h
Reserved[5]	—	1	—	[172]	—
User Area Write Protect Register	USER_WP	1	R/W, R/W/C_P, R/W/E_P	[171]	0h
Reserved[5]	—	1	—	[170]	—
FW Configuration	FW_CONFIG	1	R/W	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	20h
Write Reliability Setting Register	WR_REL_SET	1	R/W	[167]	1Fh
Write Reliability Parameter Register	WR_REL_PARAM	1	R	[166]	15h
Start Sanitize Operation	SANITIZE_START	1	W/E_P	[165]	00h
Manually Start Background Operations	BKOPS_START	1	W/E_P	[164]	00h

Enable Background Operations Handshake	BKOPS_EN	1	R/W	[163]	02h
Hardware Reset Function	RST_n_FUNCTION	1	R/W	[162]	00h
HPI Management	HPI_MGMT	1	R/W/E_P	[161]	00h
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	07h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0001D2h (For 8GB) 0003A4h (For 16GB)
Partitions Attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	00h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	00h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	00...00h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	00h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0000h
Reserved[5]	—	1	—	[135]	—
Secure Bad Block Management	SEC_BAD_BLK_MGMNT	1	R/W	[134]	00h
Production State Awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	00h
Package Case Temperature is Controlled	TCASE_SUPPORT	1	W/E_P	[132]	00h
Periodic Wakeup	PERIODIC_WAKEUP	1	R/W/E	[131]	00h
Program CID/CSD in DDR Mode Support	PROGRAM_CID_CSD_DDR_ SUPPORT	1	R	[130]	01h
Reserved[5]	—	2	—	[129:128]	—
Vendor Specific Fields [12]	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	NA
Native Sector Size	NATIVE_SECTOR_SIZE	1	R	[63]	1h
Sector Size Emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h
Sector Size	DATA_SECTOR_SIZE	1	R	[61]	0h
1st Initialization After Disabling Sector Size Emulation	INI_TIMEOUT_EMU	1	R	[60]	0Ah
Class 6 Command Control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h
Number Of Address Group To Be Released	DYNCAP_NEEDED	1	R	[58]	0h
Exception Events Control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0h
Exception Events Status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	00h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	00h
Context Configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	00...00h
Packed Command Status	PACKED_COMMAND_STATUS	1	R	[36]	0h
Packed Command Failure Index	PACKED_FAILURE_INDEX	1	R	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h
Control to Turn the Cache On/Off	CACHE_CTRL	1	R/W/E_P	[33]	0h
Flushing of the Cache	FLUSH_CACHE	1	W/E_P	[32]	0h
Control to turn the Barrier ON/OFF	BARRIEIR_CNTL	1	R/W	[31]	0h
Mode Config	MODE_CONFIG	1	R/W/E_P	[30]	0h
Mode Operation Codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h
Reserved[5]		2	—	[28:27]	—
FFU Status	FFU_STATUS	1	R	[26]	0h
Pre Loading Data Size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0000h

Max Pre Loading Data Size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	E90000h (For 8GB) 1D20000h (For 16GB)
Production State Awareness Enablement	PRODUCT_STATE_AWARENESS_ ENABLEMENT	1	R/W/E and R	[17]	01h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	3Bh
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved[5]		15	—	[14:0]	—

1. Reserved bits should be read at 0, unless otherwise specified.
2. Set to 0 after power on, hardware reset or software reset selecting backward compatibility interface timings. If the host changes the value to 1, the device will operate in high-speed mode and finally, if host changes the value to 2, HS200 interface timings will be used.
3. Set to 0 after power up and can be changed via a Switch command.
4. R = Read only.
   R/W = One time programmable and readable.
   R/W/E = Multiple writable with value kept after power failure, hardware reset assertion and any CMD0 reset and readable.
   R/W/C_P = Writable after value cleared by power failure and hardware reset assertion (the value not cleared by CMD0 reset) and readable. R/W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and readable.
   W/E_P = Multiple writable with value reset after power failure, hardware reset assertion and any CMD0 reset and not readable.
5. Value depends on state of the device.
6. Value depends on the firmware that the device is loaded with.
7. These fields are reserved for definition by the device manufacturer

Part Numbers

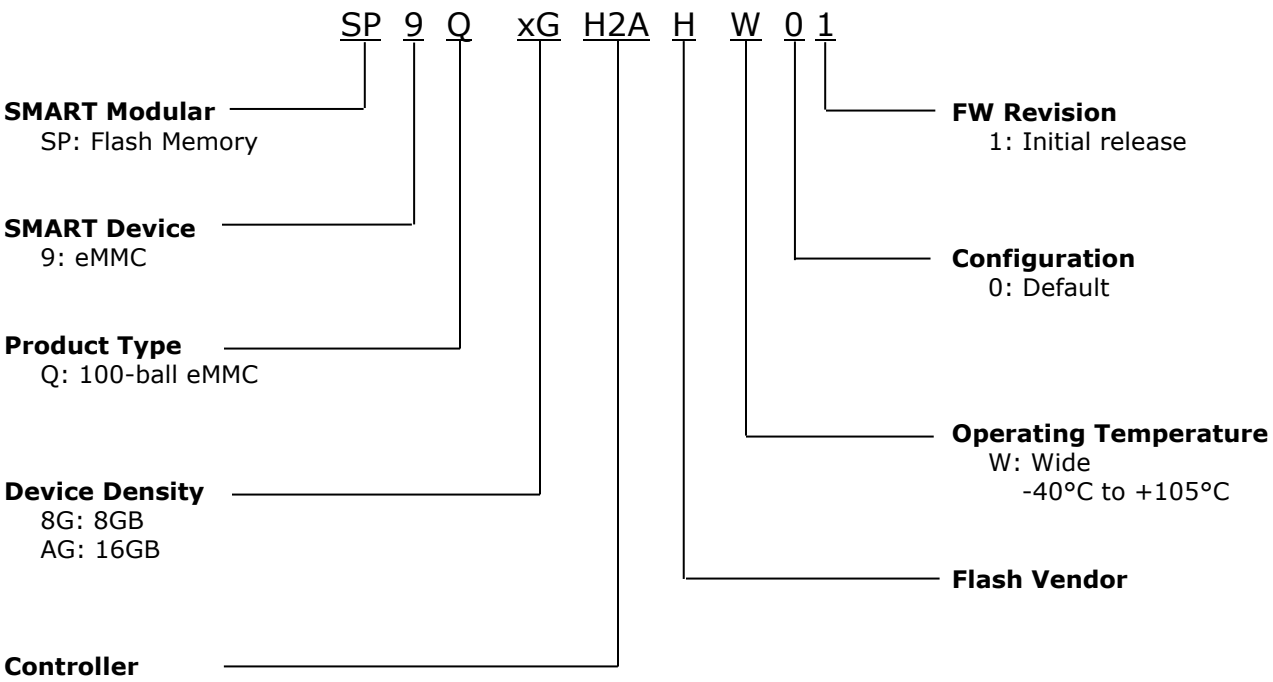
Part Numbering Information

The following table lists the available devices for this family.

Part Numbering Information

Part Number	Capacity
Wide Temperature	
SP9Q8GH2AHW01	8GB
SP9QAGH2AHW01	16GB

Part Number Decoder



Declaration of Conformity

Responsible Party Name:	SMART Modular Technologies, Inc.
Address:	39870 Eureka Drive Newark, CA 94560-4809, USA
Phone:	+1-510-623-1231

Hereby declares that the products:

SP9QxGH2AHW01

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU and its amendments

Restriction of the use of hazardous substances in electrical and electronic equipment

- **EN 50581:2012**
  Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: February 27, 2025 11:45 AM

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